

Spectroscopic charge pumping investigation of the amphoteric nature of Si/SiO₂ interface states

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The amphoteric nature of Si/SiO₂ interface states in submicron sized metal-oxide-silicon-field-effect-transistors is observed using an enhanced spectroscopic charge pumping method. The method's simplicity and high sensitivity makes it a powerful tool for interrogating the true nature of electrically measured interface states in samples which exhibit extremely low defect densities. The spectroscopic results obtained clearly illustrate a signature "double peak" density of states consistent with amphoteric P_b center data obtained from electron spin resonance measurements. Since the method is a hybrid of the commonly used charge pumping methodology, it should find widespread use in electronic device characterization. © 2011 American Institute of Physics.

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Many electron spin resonance (ESR) based studies have shown that the P_b center family of defects is responsible for interface trapping in Si/SiO₂ metal-oxide-silicon-field-effect-transistors (MOSFETs).¹⁻⁸ These studies have shown that P_b centers are silicon dangling bond defects located precisely at the Si/SiO₂ interface and exhibit an amphoteric density of states (DOS) centered around the middle of the silicon band-gap.¹⁻⁸ However, quantitative disagreements are common when comparing P_b center data obtained from ESR and Si/SiO₂ interface state data obtained from more conventional MOSFET electrical measurements.⁹⁻¹² For example, it's been argued that P_b centers account for only a small fraction of electrically measured interface states with the remaining majority due to some unknown defect.^{9,10} A potential source of the disagreements is the inability of most MOSFET electrical measurements to truly exclude the effects of noninterface defects, especially when dealing with samples of very poor quality. Thus, whether or not P_b centers account for all the "true" electrically measured interface states has been under debate for many years. A key piece of missing evidence has been the inability to electrically measure the double peak DOS response of amphoteric interface states in high quality submicron sized devices free from non-interface defect contamination.

In this work, we introduce an enhanced spectroscopic charge pumping (CP) methodology and electrically measure the DOS response of Si/SiO₂ interface states in submicron sized MOSFETs. We find that the interface state DOS is consistent with the signature double peak response expected for amphoteric P_b centers. The use of samples with extremely low defect densities ensures that noninterface defects (bulk traps) are present in negligible densities such that they have no meaningful effect on the measurement result. The

submicron sized devices serve to demonstrate the sensitivity of the method.

Electrically measuring the amphoteric nature of Si/SiO₂ interface states has previously been attempted.¹³⁻²¹ However, these attempts relied on very poor quality devices with exceedingly large interface state densities ($D_{it} > 10^{11} \text{ cm}^{-3}$). In some cases, the amphoteric nature was only observable after exposing the sample to harsh irradiation.¹⁹⁻²¹ Additionally, the devices of these studies¹³⁻²¹ almost certainly exhibit very high densities of noninterface defects which likely contaminate the measurement results. Furthermore, previous attempts based on spectroscopic CP¹⁷⁻¹⁹ have generally relied on trapped charge emission, which limits access to deep traps near midgap, while the use of complicated gate voltage pulse trains limits access to fast traps near the band-edges. In our methodology, these shortcomings have been minimized by using a simple square wave in which the CP measurement relies entirely on charge capture (rather than emission) and allows for much faster pulse rise (t_r) and fall (t_f) transition times. Together, they enable the probing of defects through midgap and allow closer access to defects near the band-edges.

Additionally, the key innovation is *choosing a CP frequency low enough to ensure complete trap filling* within the probed energy window. This last factor is generally missing in previous variable height CP based approaches, potentially leading to serious errors.

The devices used in this study are extremely high quality (consistent with production quality devices fabricated with a mature process technology) 16.45 $\mu\text{m} \times 0.24 \mu\text{m}$ n-channel MOSFETs with 5.5 nm SiO₂ gate dielectrics. CP current (I_{CP}) was measured by applying a square wave gate voltage pulse while shorting the source and drain to ground. I_{CP} was measured at the substrate with an ultralow noise current pre-amplifier and digital storage oscilloscope. Interface defects in the upper half of the band-gap are measured by fixing the

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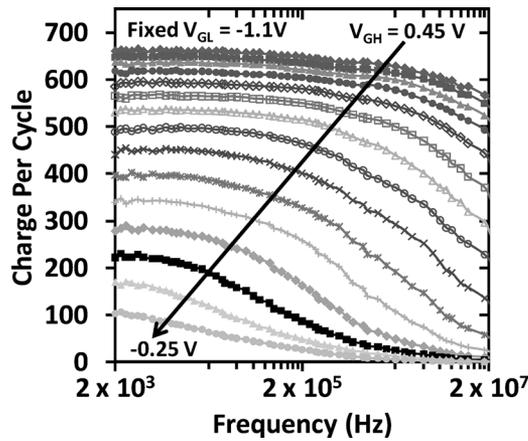


FIG. 1. The effect of insufficient interface trap filling time is illustrated by plotting charge per cycle versus CP frequency for the case of fixed accumulation. Clearly, as V_{GH} is reduced from inversion deep into depletion or the frequency is increased, an apparent loss in charge per cycle occurs. This effect must be avoided.

gate pulse low voltage (V_{GL}) at strong accumulation ($V_{GL} = -2$ V) while sequentially stepping the gate pulse high voltage (V_{GH}) from strong inversion deep into depletion. Similarly, defects in the lower half of the band-gap are measured by fixing V_{GH} at strong inversion ($V_{GH} = 1$ V) while sequentially stepping V_{GL} from strong accumulation deep into depletion. This approach is very similar to variable pulse height methods^{22,23} and allows us to obtain I_{CP} (which is proportional to the number of interface states) as a function of the probed energy window in the band-gap; enabling a count of defects as a function of energy. At each pulse bias condition, frequency dependent CP is performed at (1, 2, 3, and 4) kHz providing an easy means to correct for errors (such as gate leakage and amplifier offset) while the very low frequencies minimize (or eliminate) any incomplete trap filling issues (discussed below). CP data are then extracted at a frequency of 2 kHz. The error in absolute value of the measurements is less than 1% and the noise floor is less than 1 fA.

As previously mentioned, the key innovation is choosing a CP frequency low enough such that all available traps are given sufficient time to fill. The possibility of incomplete trap filling arises from the fact that interface trap filling time is inversely proportional to the carrier density at the interface. When the carrier density is very high (the device is held at strong accumulation or strong inversion), the traps are able to fill very quickly. Conversely, as the carrier density becomes very low (the device is biased deep into depletion) the time needed to completely fill all traps within the probed energy window can be drastically increased. Thus, ensuring that the CP frequency is low enough such that all traps within the measurement window are included is critical to an accurate and precise measurement result.

Figure 1 illustrates the detrimental effects of incomplete trap filling by comparing charge per cycle (I_{CP} divided by electronic charge and frequency) versus CP frequency for the case of fixed accumulation ($V_{GL} = -1.1$ V) and variable V_{GH} . Clearly, as V_{GH} is pushed deep into depletion and/or the frequency is increased, an apparent loss in charge per cycle occurs; this is caused by incomplete trap filling and must be avoided. As seen in Fig. 1, a CP frequency of 2 kHz avoids this effect for all but the most extreme cases. Experimentally

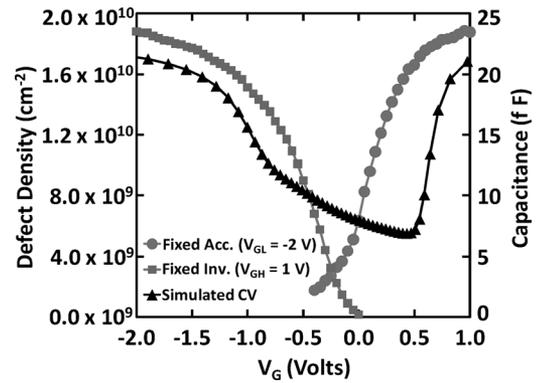


FIG. 2. I_{CP} normalized to defect density versus pulse height for the cases of fixed accumulation and fixed inversion providing a count of defects as a function of energy. Also included is a simulated CV curve.

determining the CP frequency where incomplete trap filling is avoided separates this method from conventional variable height CP which typically pays no attention to this issue and generally cannot equate “charge per cycle” to “defects per device.” The expression defects per device simply implies that complete trap filling occurs and all defects expected to participate in the CP process do actually contribute to the measured I_{CP} . At such low CP frequencies, concern may arise about bulk traps contributing to the measured I_{CP} . However, it has recently been shown that except in the case of extremely high densities, bulk defects in devices of this size generally cannot contribute.²⁴ Additionally, the use of extremely high quality samples ensures the participation of bulk traps at this quite low frequency is negligible.

Figure 2 illustrates the measured results of our approach with I_{CP} converted to defect density (left vertical axis) obtained by extracting defects per device (I_{CP} divided by electronic charge and CP frequency) at 2 kHz and dividing by the device area. The left hand data (filled squares) are for the case of fixed V_{GH} (strong inversion) and sequentially stepping V_{GL} , while the right hand data (filled circles) are for the case of fixed V_{GL} (strong accumulation) and sequentially stepping V_{GH} . Also shown is a simulated capacitance versus voltage (CV) curve. Clearly, as the pulse step height is reduced (narrowing the energy window probed in the band-gap), the total number of defects probed decreases. As previously mentioned, this is a means to count interface defects as a function of energy within the band-gap. Thus, differentiating these curves with respect to energy will provide the defect DOS.

Prestress data (filled squares) of Fig. 3 illustrate the differentiation of Fig. 2 after using the simulated CV curve to convert gate voltage (V_G) to silicon surface potential (ϕ_s). The left hand curve (extracted from fixed inversion) peaks at about 0.45 eV above the valence band-edge (VBE) and the right hand curve (extracted from fixed accumulation) peaks at about 0.76 eV above the VBE. This result, the signature double peak response centered about midgap, is consistent with the double peak response of amphoteric P_b centers obtained through ESR.¹⁻⁸ Also note the very low defect density and absolute number of defects in these devices; the amphoteric double peak signature shown here (obtained with a purely electrical measurement) on such a high quality interface has not been previously obtainable. Confirmation that the double peak response is an accurate portrayal of the in-

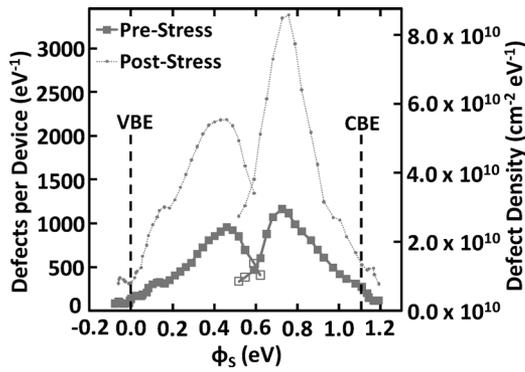


FIG. 3. Illustration of the interface state DOS obtained by differentiating the data from Fig. 2 with respect to silicon surface potential. This signature double peak response is consistent with amphoteric P_b centers.

interface state DOS is supported by the results of applying a moderate gate voltage stress ($V_G=5.5$ V for 60 s at room temperature) and repeating the measurements. The results of the stress (poststress data of Fig. 3) show that the double peak signature increases in magnitude while retaining its shape and position in the band-gap; that is, the interface state density simply increases.

Ensuring that trap filling is complete and is a key advancement made by this approach. Thus, it is very important to have a precise way to test for trap filling completeness rather than just inferring from the data shown in Fig. 1. As previously discussed, even though we extract I_{CP} data at 2 kHz only, we actually measure I_{CP} at four frequencies. Ideally, with complete interface trap filling and nonexistent bulk trap participation, the relationship between I_{CP} and frequency should be perfectly linear. Deviations from linearity indicate errors, including the onset of incomplete trap filling when one half of the CP pulse is pushed deep into depletion. This offers a way to rigorously detect incomplete trap filling by monitoring the quality of the linear fit (R^2) of the measured I_{CP} versus frequency response. For nearly all the pulse conditions shown in Fig. 2, the linear fit is perfect ($R^2=1.0$) or nearly perfect (R^2 deviates from 1.0 by less than 0.002) (not shown). However, as one half of the pulse is pushed deep into depletion (for either fixed V_{GL} or fixed V_{GH} cases) the linear fit R^2 value starts to degrade well below the above criterion (not shown). These degraded points (in Fig. 2, the three rightmost data points for fixed V_{GH} and the three leftmost data points for fixed V_{GL}) should not be trusted and are already dropped from the prestress DOS illustration of Fig. 3 (similar data have also been dropped from the poststress curve of Fig. 3). However, our differentiation routine propagates the influence of these degraded data points to the next three data points to varying degrees of severity (by the fourth point, the influence is nonexistent). Since differentiation tends to amplify small errors, the prestress data points influenced by the degraded data have, therefore, been marked with open symbols as low confidence in Fig. 3 (similar data points in the poststress curve also have low confidence).

As a check, this spectroscopic CP methodology was used to investigate an entirely different material system; SiC MOSFETs. Since interface defects in these devices are almost certainly different than those of conventional Si/SiO₂, a completely different DOS response would be expected. As discussed elsewhere,²⁵ the completely different DOS response is indeed observed which reveals the presence of four

DOS peaks. This result strongly suggests that the peak locations observed in this study are not simply measurement artifacts and represent an accurate portrayal of the defect DOS. Additionally, this demonstration highlights the usefulness and power of this methodology to study defects in other important material systems.

The simple spectroscopic CP methodology discussed provides a critical link between electrically measured Si/SiO₂ interface states with P_b center data obtained with ESR. The observed double peak signature, completely free from bulk trap contamination, should help to resolve the long standing debate regarding the true nature of Si/SiO₂ interface states. Additionally, this method could prove to be a useful spectroscopic approach to electrically interrogate interface states when studying other important material systems with much less developed understandings of their defect nature.

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- ¹P. M. Lenahan and J. F. Conley, Jr., *J. Vac. Sci. Technol. B* **16**, 2134 (1998).
- ²G. J. Gerardi, E. H. Poindexter, P. J. Kaplan, and N. M. Johnson, *Appl. Phys. Lett.* **49**, 348 (1986).
- ³P. M. Lenahan and P. V. Dressendorfer, *Appl. Phys. Lett.* **41**, 542 (1982).
- ⁴P. M. Lenahan and P. V. Dressendorfer, *J. Appl. Phys.* **55**, 3495 (1984).
- ⁵E. H. Poindexter, G. J. Gerardi, M. E. Ruckel, P. J. Caplan, N. M. Johnson, and D. K. Biegelson, *J. Appl. Phys.* **56**, 2844 (1984).
- ⁶Y. Y. Kim and P. M. Lenahan, *J. Appl. Phys.* **64**, 3551 (1988).
- ⁷M. A. Jupina and P. M. Lenahan, *IEEE Trans. Nucl. Sci.* **37**, 1650 (1990).
- ⁸N. M. Johnson, D. K. Biegelsen, M. D. Moyer, S. T. Chang, E. H. Poindexter, and P. J. Caplan, *Appl. Phys. Lett.* **43**, 563 (1983).
- ⁹E. Cartier and J. H. Stathis, *Microelectron. Eng.* **28**, 3 (1995).
- ¹⁰J. H. Stathis and D. J. DiMaria, *Appl. Phys. Lett.* **61**, 2887 (1992).
- ¹¹L. P. Trombetta, G. J. Gerardi, D. J. DiMaria, and E. Tierney, *J. Appl. Phys.* **64**, 2434 (1988).
- ¹²D. A. Buchanan and D. J. DiMaria, *J. Appl. Phys.* **67**, 7439 (1990).
- ¹³M. J. Uren, J. H. Stathis, and E. Cartier, *J. Appl. Phys.* **80**, 3915 (1996).
- ¹⁴L. A. Ragnarsson and P. Lundgren, *J. Appl. Phys.* **88**, 938 (2000).
- ¹⁵P. K. Hurley, A. Stesmans, V. V. Afanasev, B. J. O'Sullivan, and E. O'Callaghan, *J. Appl. Phys.* **93**, 3971 (2003).
- ¹⁶Y. G. Fedorenko, L. Truong, V. V. Afanas'ev, and A. Stesmans, *Mater. Sci. Semicond. Process.* **7**, 185 (2004).
- ¹⁷G. Van Den Bosch, G. V. Groeseneken, P. Heremans, and H. E. Maes, *IEEE Trans. Electron Devices* **38**, 1820 (1991).
- ¹⁸J. L. Autran, F. Seigneur, C. Plossu, and B. Balland, *J. Appl. Phys.* **74**, 3932 (1993).
- ¹⁹J. L. Autran, C. Chabrierie, P. Paillet, O. Flament, J. L. Leray, and J. C. Boudenot, *IEEE Trans. Nucl. Sci.* **43**, 2547 (1996).
- ²⁰P. B. Parchinskii, *J. Solid-State Devices and Circuits* **34**, 420 (2005).
- ²¹Y. Nishioka, E. F. da Silva, and T. P. Ma, *IEEE Trans. Nucl. Sci.* **35**, 1227 (1988).
- ²²G. Groeseneken, H. E. Maes, N. Beltran, and R. F. De Keersmaecker, *IEEE Trans. Electron Devices* **31**, 42 (1984).
- ²³J. S. Brugler and P. G. A. Jespers, *IEEE Trans. Electron Devices* **16**, 297 (1969).
- ²⁴F. Zhang, K. P. Cheung, J. P. Campbell, and J. Suehle, Proceedings of the IEEE International Reliability Physics Symposium, Anaheim, CA, 2010, p. 804.
- ²⁵J. T. Ryan, L. C. Yu, J. H. Han, J. J. Kopanski, K. P. Cheung, F. Zhang, C. Wang, J. P. Campbell, J. S. Suehle, V. Tilak, and J. Fronheiser, Proceedings of the IEEE International Reliability Physics Symposium, Monterey CA, 2011, p. 202.