The Impact of the Dielectric / Semiconductor Interface on Microstructure and Charge Carrier Transport in High-Performance Polythiophene Transistors

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The performance of organic field-effect transistors (OFETs) significantly depends on the properties of the interface between the semiconductor and gate dielectric. Here, we study the impact of chemically modified and morphologically controlled dielectrics on the performance of poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (pBTTT) semiconductors. We find that the molecular packing, domain size, and carrier mobility of pBTTT are highly sensitive to dielectric chemistry and dielectric roughness. The large and well-oriented terraced domains that are the origin of pBTTT's high performance can develop well on certain dielectrics, but can be disrupted on others.

Introduction

The choice of gate dielectric is critical to the design of organic field-effect transistors (OFETs) for flexible circuitry because it impacts both the microstructure of organic semiconductors and OFET performance (1). The chemical nature and the morphology of dielectric surfaces are especially relevant to solution-deposited semiconductors because they influence the drying and solidification process (2-8). Understanding how dielectric surface properties influence the microstructure and electrical performance of organic semiconductors is therefore a necessary first step toward the adoption of low-cost and flexible substrates, which are required to fully realize the benefits of organic semiconductors.

It has long been inferred that the chemical nature of the dielectric influences polymer semiconductor microstructure because of observations that substrate surface treatments can be used to improve charge carrier mobility (6). These observations typically include the use of clean silicon oxide, which is a widely-used model dielectric for OFETs that is conveniently available from conventional CMOS processes. Treatment of silicon oxide with hydrophobic agents, such as octyltrichlorosilane (OTS), can increase the measured charge carrier mobility by up to three orders of magnitude (1,9,10). Earlier studies on poly(3-hexylthiophene) (P3HT) (9) and poly[5,5'-bis(3-alkyl-2-thienyl)-2,2'-bithiophene] (PQT) (11) suggest that the origin of the increased mobility can be explained by morphology improvement. However, it is also recognized that polar

chemical groups on bare silicon oxide could act as traps for charge carriers, and these groups would be passivated with OTS treatment, so a separation of morphological and electrical effects has not yet been achieved (12).

The morphology of the dielectric can alter the overall order in semiconductor films. The roughness of the dielectric, in particular, is expected to strongly influence organic semiconductor microstructure because, like dielectric chemistry, it has been shown to influence the carrier mobility (13-18). Undulations in the rough surface of dielectric can act as carrier traps and also inhibit the growth of uniform, large crystal domains (1). Recent work in solution-processible polymer semiconductors such as poly(9,9-dialkylfluorene-*alt*-triarylamine) (14,19,20), regioregular poly(3-hexylthiophene) (20), and poly(2,5-bis(3-tetradecylthiophen-2-yl)thieno[3,2-b]thiophene) (pBTTT) (13) has shown that charge carrier mobility is reduced atop rougher dielectrics. For highly crystalline and high-mobility polymer semiconductors, such as polythiophene derivatives with regiosymmetric monomers (21,22), the impact of dielectric roughness on semiconductor microstructure must be established to provide guidelines for avoiding roughness-induced microstructure defects and to make the most of high-performing materials.

To study the effect of the semiconductor / dielectric interface, we employ a combination of structure analysis methods on pBTTT, a polymer semiconductor that exhibits large crystalline terraces that can extend laterally for several hundreds of nanometers after annealing in a mesophase (6,23). The molecular structure of pBTTT is shown in Fig. 1. Because pBTTT is one of a new class of high-performance polymer semiconductors that exhibit extensive 3D ordering in molecular terraces, it is an ideal material to assess the effects of different dielectric surfaces.

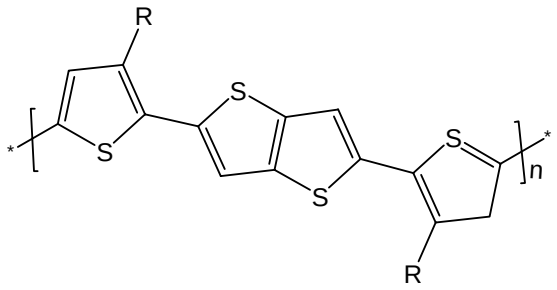

Figure 1. Chemical structure of poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-b]thiophene) (pBTTT).

We have studied the effect of dielectric chemistry by comparing bare silicon oxide to oxides hydrophobically functionalized with OTS. Roughness effects were studied with a library of variable roughness dielectrics, which were produced by exposing smooth silicon oxides to a reactive ion etch for various durations. We find that the morphology, molecular orientation, and charge carrier mobility of pBTTT depend significantly on dielectric substrate chemistry and roughness, with more significant morphological effects than previously observed for polymer semiconductors.

Experimental

Control of substrate chemistry. Silicon oxides were cleaned with an ultraviolet-ozone cleaner immediately before film deposition. OTS was deposited by immersing freshly cleaned silicon substrates in a 0.002 mol/L solution of OTS in anhydrous hexadecane for 12 h. Samples were then ultrasonically cleaned in baths of chloroform, isopropanol, and de-ionized water.

Polymer semiconductor film preparation. The pBTTT films were deposited by spin-casting from a 5 mg/ml solution in 85 °C 1,2 dichlorobenzene or a 4 mg/mL solution in 80 °C 1,2 dichlorobenzene and chloroform mixture with 8:1 volume ratio. Films were cast at 1500($\cdot 2\pi$) rad/min using a 100($\cdot 2\pi$) rad/min s ramp rate for the dichlorobenzene solution or 3000($\cdot 2\pi$) rad/min for the solution mixture. Films were then heated on a hot plate (180 °C) for 5 min, followed by a slow cool ($\approx$ 10 °C/min).

Creating substrate roughness. To create rough gate dielectric layers, a series of rough oxides were prepared with a reactive ion etching (RIE) tool, Silicon RIE Unaxis-790 (Unaxis Wafer Processing, St. Petersburg, FL) located in the National Institute of Standards and Technology (NIST) nanofab facility (24). Initially smooth, 200 nm thermally grown oxides (RMS roughness is $\approx$ 0.2 nm) on highly n-doped silicon wafers were etched. During the etching process, CF_4 etching gas was supplied constantly at 40 sccm, the pressure inside the chamber was kept at 13 Pa, and the power was 100 W which provides an etching rate of 20 nm/min.

Structural characterization. Topographical images of each substrate were obtained with atomic force microscopy (AFM: Dimension 3100, Veeco) performed in tapping mode with silicon cantilevers (Nanosensors). Near edge X-ray absorption fine structure (NEXAFS) spectroscopy was performed at NIST beamline U7A of the National Synchrotron Light Source (NSLS) of Brookhaven National Laboratory. Carbon K-edge collection was performed in partial electron yield (PEY) mode with a grid bias of -50 V. Spectra collected at various incident angles, Θ, from 20° to 90° and were normalized with respect to carbon concentration by their intensity at 330 eV. Specular X-ray diffractions were performed on beamline 2-1 at the Stanford Synchrotron Research Laboratory and were also conducted using a laboratory-scale small-angle X-ray scattering instrument (Rigaku) with Mo $K_{\alpha 1}$ radiation in conventional pinhole geometry. A PerkinElmer Lambda 950 UV-Vis spectrometer was used to measure the absorption spectrum.

Electrical test. Bottom contact thin film transistors (TFTs) were fabricated by depositing gold/titanium (45 nm/5 nm) electrodes on oxidized, highly doped, ⟨100⟩ silicon wafers with 200 nm oxide. Top contact source and drain gold electrodes were thermally evaporated on top of the pBTTT through a shadow mask. Pressure inside the chamber of the evaporator was maintained under 133 mPa and the electrodes were deposited to 60 nm with a deposition rate of 0.05 nm/s. I-V measurements were performed in a Cascade Microtech probe station. In a plot of the square root of the drain current versus gate voltage, we fit the data in the saturation regime. All polymer processing and measurements were performed in nitrogen.

Results and Discussion

Effect of dielectric chemistry

The starting point in evaluating the effect of dielectric chemistry on pBTTT microstructure was to image the film surface morphology. AFM images of thin pBTTT films clearly reveal differences in terrace formation atop the different substrate surface chemistries. After heating pBTTT with dodecyl side chains to a mesophase (≈ 180 ºC) and then cooling, pBTTT films exhibit the terraced microstructure shown in Fig. 2. On the OTS functionalized oxide, the lateral terrace size is much larger than that on the bare oxide, with nearly micron-sized domains on OTS and ≈ 100 nm domains on oxide. All as-cast films show no terracing and appear similar independent of substrate. Even though pBTTT terrace formation is more developed after heating on oxide, the charge carrier mobility is significantly higher in the as-cast film, as shown in Table 1. The decrease in mobility after heating may be due to the apparent grain boundaries created during terrace formation. Grain boundaries in low molar mass P3HT have been shown to be detrimental to charge carrier mobility (25).

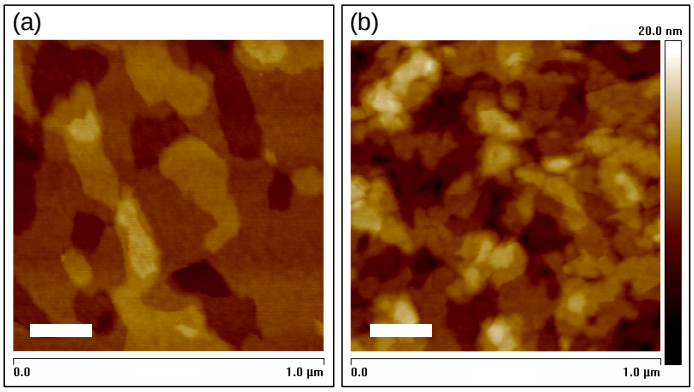

Figure 2. AFM images comparing microstructure of pBTTT on OTS (a) and oxide (b). Scale bar denotes 200 nm.

TABLE I. Charge carrier mobilities for oxide and OTS treated oxide substrates. Data are reported with the standard uncertainty (6).

Substrate	$\mu_{as\text{-}cast}$ ($cm^2 V^{-1} s^{-1}$)	μ_{anneal} ($cm^2 V^{-1} s^{-1}$)
Oxide	0.10 ± 0.02	0.03 ± 0.01
OTS	0.12 ± 0.02	0.27 ± 0.05

Terrace formation increases the Bragg scattering intensity of specular X-ray diffraction (XRD) (6) (results not shown here). For both the oxide and OTS substrates, the width of the diffraction peaks decreases, and the same lamellar spacing is observed after heating. The domain size normal to the substrate, as estimated by the Scherrer relationship, is approximately equal to the film thickness. This result suggests that while the oxide dielectric chemistry limits lateral pBTTT terrace size, it does not disrupt overall order along the surface normal. In contrast, NEXAFS spectroscopy shows similar pBTTT π-plane orientation in both as-cast films, but the orientation improves after

heating only on the OTS substrate (6). NEXAFS measures the average orientational order of the conjugated plane including amorphous regions, while XRD measures the lamellar stacking along surface normal. The greater number of grain boundaries after heating atop oxide may be responsible for the decreased orientational order.

The increased number of grain boundaries in pBTTT on oxide may be a result of higher nucleation density, with the smaller islands resulting from a stronger interaction between the substrate and the film. According to AFM, the oxide surfaces are actually somewhat smoother than OTS treated surfaces. So it seems likely that the nucleation sites have a chemical rather than topographical origin. We speculate that reactive groups on the oxide chemically pin molecules to the surface, which serve as nucleation sites. Such a mechanism would likely involve an interaction between surface reactive groups and the aromatic rings of the pBTTT backbone. Because NEXAFS reveals no comprehensive change in the chemistry or orientation of pBTTT, it seems likely that such pinning occurs very sporadically and not in a comprehensive monolayer. It remains ambiguous whether the decrease in charge carrier mobility after heating on oxide stems entirely from the disrupted morphology or whether trap states also contribute, but these results provide unambiguous proof that a morphological impact does occur.

Effect of dielectric roughness

To examine the effect of substrate roughness on the polymer semiconductor, a series of dielectrics with six different RMS roughness values were prepared by RIE on thermally grown silicon oxides. This roughness library varied in RMS roughness from 0.3 to 3.0 nm after OTS passivation. Figure 3a-d show AFM micrographs of the roughened oxides.

The micron-scale terraces of pBTTT films on flat surfaces, as shown in Fig. 2a, are disrupted by solidification on the rough substrates. AFM micrographs of pBTTT with tetradecyl side chains cast on the roughened dielectrics after heating to a mesophase (≈ 180 °C) are shown in Fig. 3e-h. Terraces atop the flattest dielectric (Fig. 3e) exhibit ≈ (100 to 400) nm lateral size on the film surface (6,23). As dielectric roughness increases, however, a significant detrimental morphology change in the pBTTT layer is observed (4). Domain size decreases (Fig. 3f) and films atop dielectrics with RMS roughness greater than 0.78 nm exhibit no terraces (Fig. 3g and h). Interestingly, there appears to be a critical RMS roughness between 0.53 nm and 0.78 nm where domain formation is disrupted. This critical roughness is similar to the threshold roughness required to decrease carrier mobility in amorphous poly(9,9-dialkyl-fluorene-alt-triarylamine) (14,19). This critical RMS roughness implies that there exists a condition at which pBTTT domains can no longer remain intact while conforming to the substrate. In AFM images of rough substrates, we can collect information about the magnitude of local nanoscale curvature, although the radius of curvature might be overestimated due to convolution with the AFM tip, especially for the roughest films where the tip shape appears to be present in the image. Higher-amplitude roughness at longer lateral length scales may not impact pBTTT microstructure provided that the radius of curvature is large. This result has important implications for the application of pBTTT to plastic substrates and polymer dielectrics, because it places stringent constraints on the acceptable dielectric morphology.

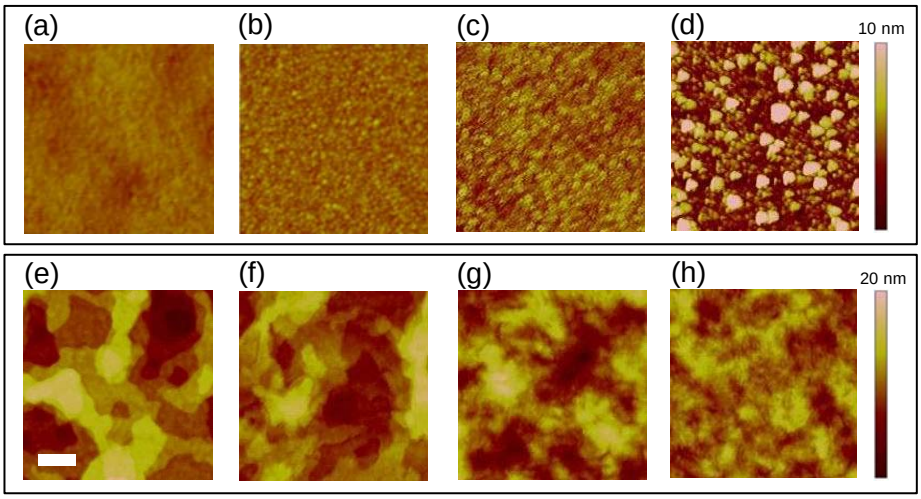

Figure 3. (a) – (d) AFM micrographs of rough oxides after OTS passivation. All images have 10 nm vertical scales. RMS roughness of (a) = 0.33; b) 0.53; c) 0.78; d) 3.04 nm. (e) – (h) AFM of pBTTT atop each rough surface after heating above mesophase transition and then cooling. All images have 20 nm height scales and are 1 μm × 1 μm size. Scale bar denotes 200 nm (4).

Although clear dielectric-induced morphological changes in pBTTT semiconductors are revealed by AFM, there is no profound change in the molecular-scale packing within domains and the overall molecular orientation confirmed by UV-Vis absorption and NEXAFS spectroscopy, respectively. The π-orbital delocalization improves upon annealing to a similar extent regardless of roughness, and rough dielectrics do not substantially impact the pBTTT molecular orientation, although orientation may be modestly disturbed on very rough dielectrics. However, long range positional order along the surface normal, as evaluated with specular XRD (26), is evidently affected by the substrate roughness.

Figure 4a shows the (200) Bragg peaks of pBTTT films, from the scattered intensity along the vertical q_z axis. Sharp peaks in each Bragg peaks are from the beam reflections. Figure 4b shows rocking curves about the (200) Bragg peak, from the intensity along the horizontal q_{xy} axis. The Bragg peak intensity decreases substantially for the pBTTT film on the roughest dielectric (3 nm), but the peak does not substantially broaden along the q_z or q_{xy} axes. The vertical peak width result of the broad Bragg peaks along q_z indicates that the diffracting layered domains extend vertically to the entire pBTTT film thickness. The horizontal peak width result along q_{xy} indicates that the lateral coherence of the diffracting crystals is similar for all films. The reduction in peak intensity for the films atop the roughest dielectrics indicates that large portions do not have long-range order and therefore do not contribute to the diffraction. It is also found that there is not a significant population of tilted layers in the annealed pBTTT film on any rough substrate. This result does not contradict the UV-Vis spectroscopy finding that roughness does not profoundly impact the molecular-scale packing or conformation of the pBTTT chains, because the UV-Vis absorption measurement evaluates interactions between neighbouring chains within layers, whereas the XRD measurement evaluates longer-range order among multiple layers. Further, this XRD result also agrees with the

NEXAFS analysis, which indicated negligible domain tilt regardless of dielectric roughness.

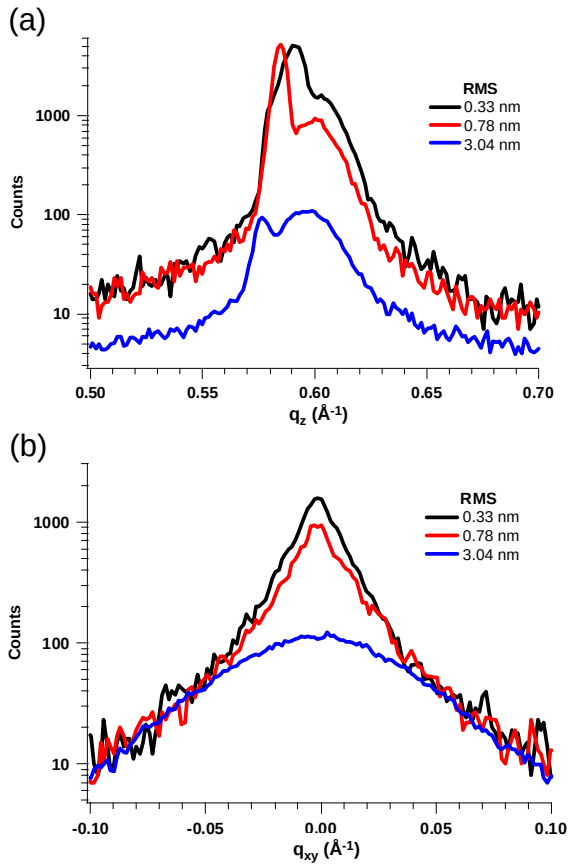

Figure 4. X-ray diffraction of annealed pBTTT on various roughness OTS treated substrates. (a) q_z and (b) q_{xy} of the (200) diffraction obtained from two-dimensional diffraction images near the Bragg condition (4).

Combining the results of the AFM, spectroscopy, and XRD studies, we find that there is a substantial decrease in the lateral size of crystals on rough dielectrics and an increase in the number of areas with poor intermolecular interaction between domains. Therefore, a strong dependence of charge carrier mobility on the interfacial roughness is expected. Typically, the hole mobility of pBTTT films increases by a factor of (1.5 to 2) after heating above the mesophase transition and then cooling (6,21). The hole mobility of as-cast films was similar for all dielectric roughnesses in the (0.002 to 0.02) $cm^2\ V^{-1}\ s^{-1}$ range, but exhibited a clear dependence on dielectric roughness after heating, as shown in Fig. 5. Increasing dielectric roughness causes a substantial reduction of the hole mobility. Mobility falls most dramatically at 0.78 nm RMS roughness where microscopy indicates that terraces are disrupted (Fig. 3). The mechanism of mobility decrease in pBTTT on rough dielectrics is likely due to the combination of an increased number of lateral grain boundaries, which will limit transport between domains, and an increased number of packing defects which will limit transport within domains.

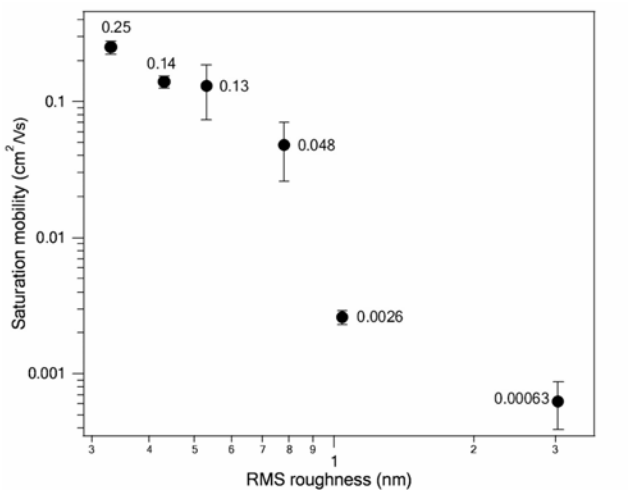

Figure 5. Charge carrier mobility (μ) plot for pBTTT thin film transistors after heating at mesophase for substrates of various dielectric roughness. Uncertainty in mobility measurements is the standard deviation calculated from the distribution of saturation field effect mobilities.

Conclusion

We have studied the impact of dielectric chemistry and dielectric roughness on semiconductor morphology and OFET performance. Our results show all parameters can influence the carrier mobility of high-performance polymer OFETs.

The chemical nature of the dielectric can alter the pBTTT domain size. On oxides hydrophobically functionalized with OTS, the lateral domain dimensions of pBTTT are approximately 10 times larger than those that form on bare silicon oxide surfaces. The field effect mobility is also correspondingly higher on OTS-functionalized surfaces. The difference appears to be caused by a greater nucleation density on the bare oxide.

The roughness of the dielectric can alter the overall order in pBTTT films. Dielectric surfaces with RMS roughness greater than 0.5 nm exhibit significant changes in the morphology of the pBTTT active layer and large reductions in charge carrier mobility. Rough dielectrics, even if they are OTS-functionalized, alter the layered pBTTT microstructure by reducing lateral domain size and decreasing the extent of long-range layer order. Even a small interfacial roughness with a spatial frequency less than the nominal domain size can severely compromise the performance of pBTTT OFETs.

Dielectric chemistry and dielectric roughness can all influence the carrier mobility of high-performance polymer OFETs. These results provide practical guidelines, supported by fundamental measurements of the dielectric, semiconductor, and interface, to support flexible device design for this exciting new class of polymer semiconductors.

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