

Electrical Methods for Mechanical Characterization of Interconnect Thin Films

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ABSTRACT

We describe the use of electrical methods for evaluating mechanical reliability and properties of patterned copper and aluminum interconnects on silicon substrates. The approach makes use of controlled Joule heating, which causes thermal strains in the materials system due to differences in thermal expansion between the metal and constraining substrate and passivation. Our efforts concentrate on understanding damage formation in the interconnects and on the development of meaningful test methods. We make use of alternating currents in a frequency range (100 Hz to 10 kHz) that does not lead to electromigration but instead causes extensive thermal fatigue damage and failure in the metal interconnects.

INTRODUCTION

The development of measurement methods for the mechanical response of crystalline materials with constrained dimensions has seen considerable attention in the past decade. This is due to the observation that such materials generally do not exhibit behaviors easily predictable from the behaviors of the same materials in bulk form. In particular, methods such as microtensile testing of free-standing films [1] and nanoindentation of films on substrates [2] are often utilized for measuring properties such as strength, hardness, or ductility. While valuable, these methods are sometimes viewed as cumbersome in terms of implementation and interpretation, due to specimen preparation that is not trivial or property extraction that is not straightforward. In the case of fatigue of thin films, microtensile approaches have been shown to be useful for studies of non-passivated films [3, 4], though they prove difficult to apply to cyclic deformation in the case of very narrow or passivated structures.

A recent paper [5] has demonstrated that application of alternating currents may offer a viable alternative to purely mechanical methods for measuring thermal fatigue in patterned interconnects. The method makes use of a.c. at high current density, in the frequency range 100 Hz to 10 kHz. Under such conditions, the period is short enough to preclude electromigration since there is insufficient time for net diffusion to occur during a power cycle. On the other hand, the frequency is slow enough to allow for considerable Joule heating to occur within each power cycle. Mismatch in coefficient of thermal expansion (CTE), $\Delta\alpha$, between substrate and film then leads to cyclic strain, ε , at twice the a.c. frequency:

$$\varepsilon = \Delta\alpha\Delta T \quad (1)$$

where ΔT is the temperature change induced during one power cycle. Cyclic strain applied in this manner was shown to lead to thermal fatigue damage in the interconnects.

An electrical approach to thermal fatigue testing also offers several advantages over the commonly used method of thermal cycling coupled with wafer curvature measurement. Any patterned structure with electrical access can be tested, including those with dimensions below 1 μm . Buried structures may be tested. Thermal strains are induced by the materials system associated with the structure of interest, in a more realistic device configuration. Tests can be conducted rapidly, incorporating lifetime monitoring using failure criteria such as resistance changes. Disadvantages of the electrical approach at present include more uncertainty in applied temperatures and indirect knowledge of strain and stress response. This approach becomes less effective at frequencies much in excess of 10 kHz.

We present in this paper detailed observations of the evolution of surface and microstructure damage as a function of accumulated cycles in copper and aluminum interconnects on silicon substrates. We also discuss the applicability of electrical methods to assessment of mechanical properties such as strength and ductility.

EXPERIMENT

Materials

Al-1Si (weight percent) was sputtered onto oxidized Si substrates using conventional processing parameters. We used a non-passivated, single level NIST-2 test structure originally designed for electromigration and thermal conductivity measurements. The lines were 800 μm long, 3.3 μm wide, 0.5 μm thick and exhibited a strong $\langle 111 \rangle$ fiber texture. The resulting grains were columnar with a mean diameter of approximately 1.4 μm .

Cu lines of length 800 μm , width (8 to 15) μm , and thickness (100 or 300) nm were fabricated by sputter deposition and lift-off processing. A 5 nm Ta adhesion layer was present between the lines and the oxidized Si. After fabrication, these samples were annealed in vacuum at 400 °C for 15 h to allow for grain growth and microstructure stabilization. The resulting grains were heavily twinned and columnar with a mean diameter of approximately 0.3 μm and 1.5 μm for the thin and thick Cu lines. The lines exhibited a predominantly $\langle 111 \rangle$ fiber texture with a small $\langle 100 \rangle$ component.

Test Procedure

Specimens were tested on a 4-point probe station using sinusoidal alternating currents with frequency in the range 100 Hz to 10 kHz, following details as discussed in reference [5]. Current densities (rms) ranged from (6 to 30) MA/cm^2 . For the Al-1Si experiments, the test chip was held in place on a large steel stage during testing using a vacuum chuck. For Cu, the test chip was held in place on a smaller steel stage for testing within the vacuum chamber of a scanning electron microscope (SEM), in order to minimize oxidation. Lifetime tests were conducted continuously until the test lines became electrically open. The average temperature was estimated along the length of each line by use of time-resolved resistance measurements. Localized measurements of temperature were made on Al-1Si specimens by use of a scanning thermal microscope (SThM). We followed the evolution of microstructure during the course of several tests on the lines by use of field emission SEM and automated electron backscatter

diffraction (EBSD). Transmission electron microscopy (TEM) was also used to observe defect structures.

RESULTS AND DISCUSSION

Temperature Measurement

Critical to the successful use of thermal strains induced by electrical stressing is reliable knowledge of the temperatures applied to a test structure. Chip temperatures can be measured by use of a thermocouple attached to the chip; such measurements indicate the time-averaged temperature of the whole chip, but do not resolve the maxima and minima. The average temperature along the length of a line can be determined during a test, by means of time-resolved measurements of resistance. A digital oscilloscope can be used to record voltage and current as a function of time. Since resistance and temperature of a metal have a linear relationship the time resolved temperature can be determined. This process was used to plot maximum and minimum temperature against applied peak power in reference [5] for Cu, with a temperature uncertainty of 3 °C. As an example, for an applied peak power of 6 W, the maximum temperature experienced by a line was approximately 300 °C and the minimum was approximately 125 °C.

We have made progress in time-resolved measurements of temperature with higher spatial resolution as well. This is done by use of a SThM, where the probe tip acts as either a point-source heater or a resistive element in a Wheatstone bridge circuit. In this manner, we obtained a plot of thermal voltage (proportional to temperature, with a suitable calibration) against time, for an Al-1Si line subjected to 7 MA/cm² rms current, as shown in figure 1. The plot shows temperature variation for a single position of the SThM probe, over 0.2 s, for a 10 Hz current; the oscillation is approximately 25 °C. At present, we are limited to low frequencies for this measurement, but anticipate instrumentation improvements to enable faster data collection. Figure 2 shows a thermal SThM image corresponding to the time-resolved data shown in figure 1. Darker intensities imply higher temperature; the bright horizontal lines are a scanning artifact.

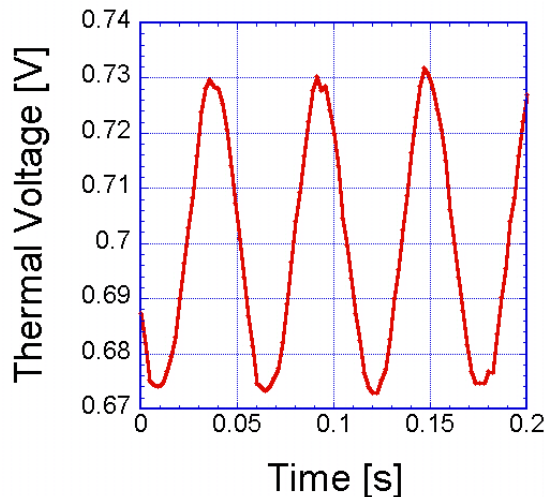


Figure 1. Thermal voltage versus time for Al-1Si (weight percent) line undergoing 7 MA/cm² rms a.c. stressing; the temperature oscillation is approximately 25 °C.

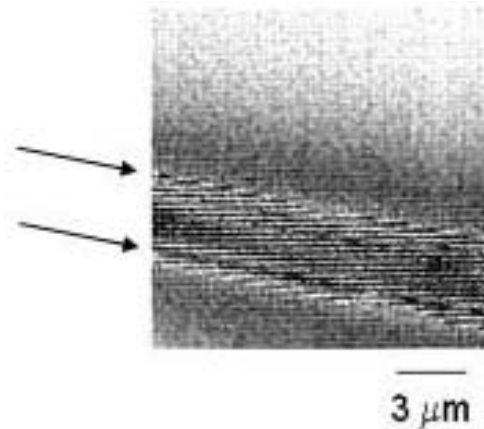


Figure 2. SThM image showing temperature distribution associated with line described in figure 1. Darker intensity implies higher temperature. Bright horizontal lines are a scanning artifact. Arrows indicate line edges.

The arrows indicate the edges of the line. We note that the original data of this figure is represented on a thermal color scale, so the grayscale reproduction for this paper is somewhat inaccurate. The image shows that the interconnect is warmest, and the temperature decreases rapidly away from the line. The ambient chip temperature is reached within less than 10 μm from the interconnect. Further studies are underway to image local hot spots due to geometry changes.

Thermal Fatigue Damage in Copper and Aluminum Interconnects

We describe the evolution of surface and microstructure damage in Cu and Al-1Si lines. In general, both materials showed the development of severe topography and grain growth; Al-1Si additionally exhibited grain re-orientation. Figure 3 shows SEM images of the topography that forms, likely as a result of dislocation slip processes. Early in the tests, the surface damage tended to be confined to selected areas of the lines. EBSD mapping indicated such areas to be individual grains. With continued cycling, the sizes of the damaged regions increased. EBSD mapping also revealed that the growth of such regions could be correlated to the growth of grains for both metals. Figure 4 shows an example of grain growth in Cu after 8.4×10^5 cycles at $\Delta T = 180^\circ\text{C}$. The large rectangular-shaped region grew during cycling predominantly in a $\langle 001 \rangle$ orientation, with a small angle grain boundary as indicated by the arrow. In the Cu lines, grain growth was preceded by the dissolution of grown-in twins early during testing [6].

Figure 5 shows an example of grain growth in Al-1Si. This figure shows the evolution of grain structure after 1.6×10^4 cycles at $\Delta T = 100^\circ\text{C}$. The orientation maps show both grain growth and re-orientation. In fact, we were able to track the re-orientation of many grains that also showed extensive surface damage. The orientations changed from the initial $\langle 111 \rangle$ by as much as 35° or more, generally towards the $\langle 112 \rangle$. Such changes appear to be consistent with slip asymmetry during the constrained cyclic deformation of face-centered cubic crystals [7].

Surface damage appears to be strongly tied to a combination of grain size, grain orientation, and grain boundary structure. In the aluminum alloy, we suggest that regions that become heavily deformed begin from grains that are initially weaker (i.e. larger grain diameter), have a large resolved shear stress on them (i.e. large Schmid factor), and have boundaries that are active

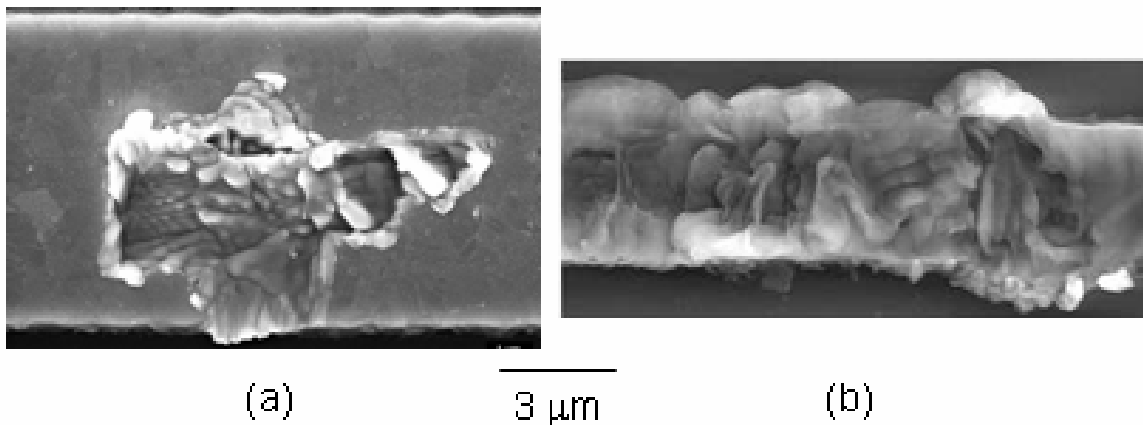


Figure 3. Surface damage induced by thermal fatigue in: (a) Cu, after 2.2×10^6 cycles at $\Delta T = 150^\circ\text{C}$; film thickness = 300 nm, and (b) Al-1Si, after 1.4×10^5 cycles at $\Delta T = 100^\circ\text{C}$. Images are shown at same magnification.

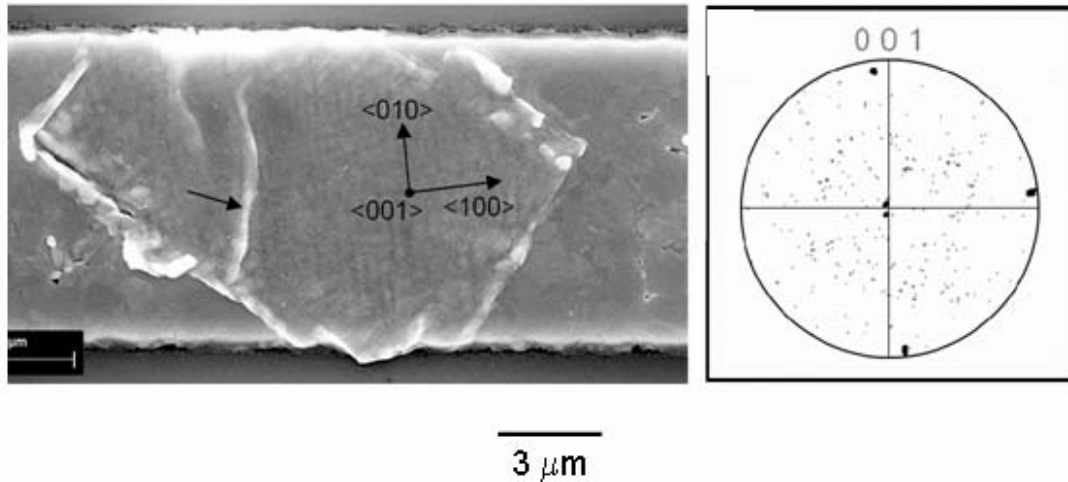


Figure 4. Example of grain growth in Cu, with corresponding (001) pole figure. Arrow at far left indicates a low angle grain boundary. Line was tested for 8.4×10^5 cycles at $\Delta T = 180$ °C.

sources of dislocations. The process was sometimes self-sustaining: initially favorable sites for damage became more favorable, as they grew and re-oriented. A similar argument can be made for copper, with the exception that damage appeared in $\langle 001 \rangle$ grains before $\langle 111 \rangle$ grains, despite the former showing a small Schmid factor. It has been suggested [6] that first generation $\langle 112 \rangle$ twins may contribute to this, as the $\langle 112 \rangle$ orientation experiences a larger resolved shear stress than $\langle 111 \rangle$.

Implications on Interconnect Reliability

We discuss here some implications of our studies on the reliability of patterned interconnects that undergo large numbers of thermal cycles. Our observations suggest that Cu withstood more cycles at higher thermal strains than Al-1Si, as measured by the severity of the topography. This is due to the fact that Cu was deformed at a relatively low homologous temperature compared to Al-1Si and suggests that the Cu deformed by means of a low temperature mechanism such as dislocation glide. Al-1Si deformed by means of a higher

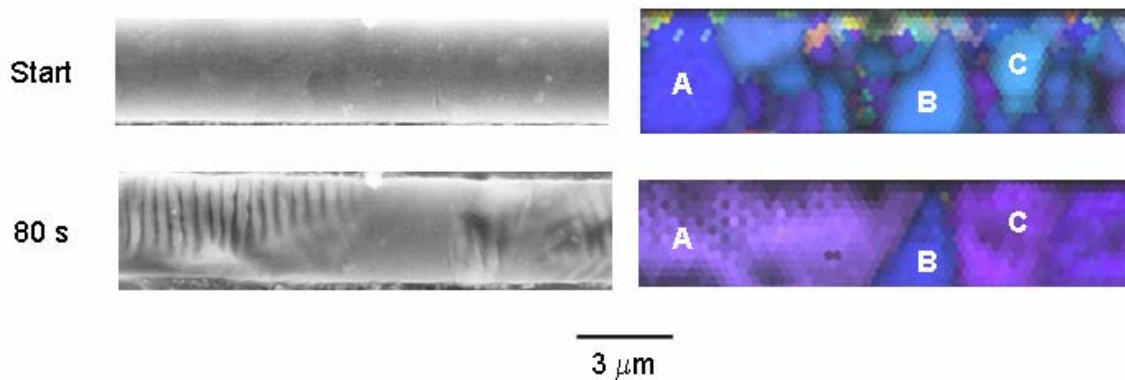


Figure 5. Grain growth in Al-1Si. Left SEM images show surface structure, and right EBSD maps show grain structure. Upper pair represents line prior to testing. Lower pair represents line after 80 s (1.6×10^4 cycles) at $\Delta T = 100$ °C. Letters indicate same locations before and after test.

temperature mechanism, with enhanced point defect mobility contributing to the glide processes. TEM studies supported this idea through observations of a high density of prismatic loops in the Al-1Si, suggesting high densities and mobilities of lattice vacancies.

We observed a film thickness effect for the case of copper. Thinner (100 nm) films withstood higher thermal strains than the thicker (300 nm) films. For a given number of cycles, the 100 nm films could undergo testing at a temperature amplitude of nearly 100 °C more than the 300 nm films, as determined by lifetime measurements [6]. This was attributed to a transition from dislocation- to diffusion-controlled deformation due to the inhibition of dislocation nucleation and motion in thinner films [2].

Finally, the formation of severe surface topography was observed to occur even in the presence of a relatively soft overlayer [8]. Hard-baked photoresist was shown to provide no significant resistance to the formation of topography such as that shown in this paper.

Measurement of Mechanical Properties by use of Electrical Methods

We are in the process of exploring how electrical methods can be used to measure other mechanical properties of thin films and interconnects. One approach is to determine the fatigue strength coefficient in the Basquin Law by extrapolating back to a half cycle to failure on a stress-lifetime plot. This factor correlates well to ultimate strength, particularly for purer metals. Measurements of residual resistivity, which is the temperature-independent contribution to total resistivity of a metal per Matthiessen's Rule, may be an important indicator, although this is not yet established. Combined with SEM imaging this method might be used either to detect dimensional changes or to measure changes in the defect concentrations in interconnects.

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REFERENCES

1. F. R. Brotzen, *Int. Mater. Rev.* **39**, 24-45 (1994).
2. W. D. Nix, *Mater. Sci. Eng.* **A234**, 37-44 (1997).
3. N. Barbosa, P. El-Deiry, and R.P. Vinci in *Thin Films - Stresses and Mechanical Properties X*, edited by S. G. Corcoran, Y. -C. Joo, N. R. Moody, and Z. Suo, (Mater. Res. Soc. Proc. **795**, Pittsburgh, PA, 2004) pp. 423-428.
4. R. Schwaiger and O. Kraft, *Acta Mater.* **51**, 195-206 (2003).
5. R. Mönig, R. R. Keller, and C. A. Volkert, *Rev. Sci. Instrum.* **75**, 4997-5004 (2004).
6. R. Mönig, *Thermal Fatigue of Cu Thin Films*, Ph.D. Dissertation, Universität Stuttgart (2004); <http://elib.uni-stuttgart.de/opus/volltexte/2005/2173>.
7. S. X. Li, X. W. Li, Z. F. Zhang, Z. G. Wang, and K. Lu, *Philos. Mag.* **82**, 3129-3147 (2002).
8. R. R. Keller, R. Mönig, C. A. Volkert, E. Arzt, R. Schwaiger, and O. Kraft in *Stress-Induced Phenomena in Metallizations: 6th Int'l. Workshop*, edited by S.P. Baker, M.A. Korhonen, E. Arzt, and P.S. Ho, (AIP Conf. Proceedings **612**, Melville, NY, 2002) pp. 119-132.