Broadband Lumped-Element Integrated N-Way Power Dividers for Voltage Standards

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***Abstract*—This paper presents a monolithically integrated broadband lumped-element Wilkinson power divider centered at 20 GHz, which was designed and fabricated to uniformly distribute power to arrays of Josephson junctions (JJs) for superconducting voltage standards. This solution achieves a fourfold decrease in chip area, and a twofold increase in bandwidth (BW) when compared to the previous narrowband distributed circuit. A single Wilkinson divider demonstrates 0.4-dB maximum insertion loss (IL), a 10-dB match BW of 10–24.5 GHz, and a 10-dB isolation BW of 13–30 GHz. A 16-way four-level binary Wilkinson power divider network is characterized in a divider/attenuator/combiner back-to-back measurement configuration with a 10-dB match BW of 10–25 GHz. In the 15–22-GHz band of interest, the maximum IL for the 16-way divider network is 0.5 dB, with an average of 0.2 dB. The amplitude balance of the divider at 15, 19, and 22 GHz is measured to be $\pm$1.0 dB utilizing 16 arrays of 15 600 JJs as on-chip power detectors.**

***Index Terms*—Cryogenic electronics, Josephson arrays, lumped-element microwave circuits, microwave integrated circuits (ICs), power dividers, superconducting coils, superconducting ICs, superconducting microwave devices.**

I. Introduction

THIS PAPER addresses the design, analysis, and testing of superconducting microwave integrated-circuit (IC) lumped-element Wilkinson power dividers for a programmable Josephson voltage standard [1]. On-chip power division is needed to enable multiple arrays of many Josephson junctions (JJs) periodically loading coplanar waveguide (CPW) transmission lines in niobium (Nb) on a silicon (Si) substrate [2]. The goal of the current research is to utilize a monolithically integrated 16-way power divider to excite $\sim$ 250 000 junctions at 20 GHz producing a 10-V programmable Josephson voltage standard [3]. The present National Institute of Standards and Technology (NIST) programmable Josephson voltage standard systems are limited to 1 V without on-chip power division. The scale of the inverse of the Josephson constant, ${}^{1}/_{K_{J-90}} = 2.067834\ \mu$V/GHz per junction, drives the increase in frequency and number of junctions to achieve the higher output voltage [1].

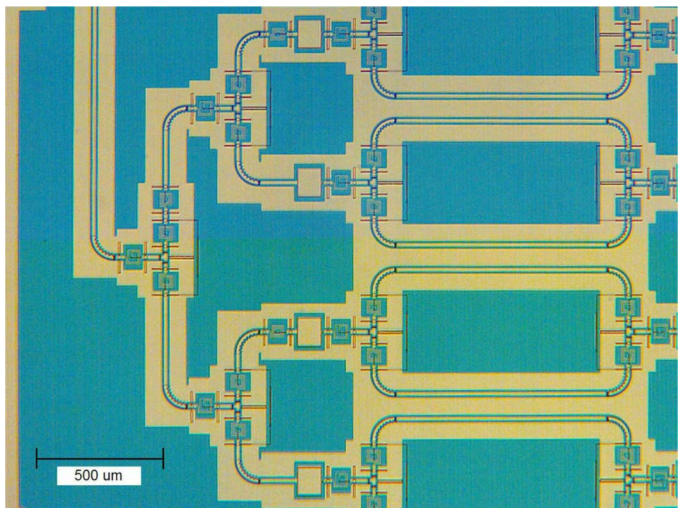

Fig. 1. Micrograph of a portion of the broadband balanced 16-way divider/combiner configuration. Three binary levels of power division utilizing the 20-GHz lumped-element Wilkinson divider are shown. The light colored yellow material (in online version) is Nb, the darker blue material (in online version) is the Si substrate.

The superconducting Nb used for the junctions gives the IC designer the advantage of creating complex low-loss circuits using integrated superconducting CPW transmission lines, high-quality inductors, and very low series resistance capacitors [4]. This enables broadband lumped-element Wilkinson power dividers with very low loss, compact size, and broad bandwidth (BW) compared to commercial and published dividers in CMOS, stripline, and other technologies [5]–[10]. Fig. 1 is a micrograph showing a section of a fabricated Wilkinson divider test circuit with a design frequency of 20 GHz and BW in excess of 10 GHz.

Here, the design of a lumped-element Wilkinson divider unit cell is presented, followed by a discussion of fabrication, and then cryogenic measurement results are shown from 10 to 30 GHz. Next, a four-level binary balanced divider utilizing these unit cells was designed to meet the challenge of increasing the number of junction arrays under parallel microwave excitation on a chip. Cryogenic measurements are performed on the 16-way Wilkinson divider in a back-to-back divider/10-dB attenuator/combiner configuration. This configuration preserves the desired matched-load N-way divider in a two-port through test circuit suitable for insertion-loss measurements. A

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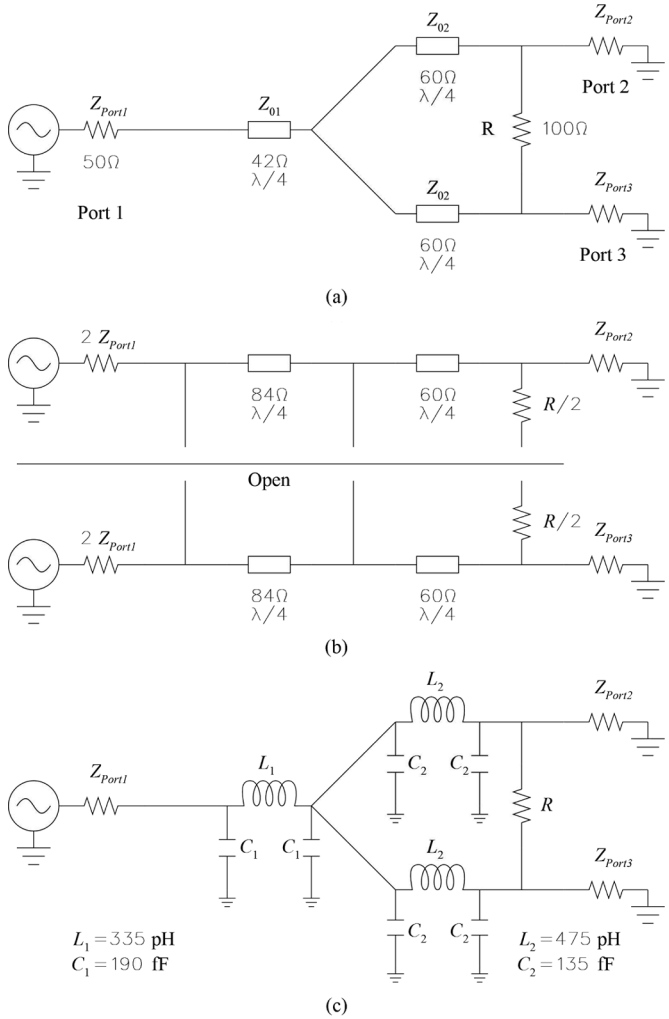

Fig. 2. 20-GHz broadband Wilkinson power divider circuit schematics. (a) Distributed 50-Ω input and output impedance divider. (b) Forward even-mode divider half-circuit Butterworth transformers. (c) Divider with $\lambda/4$ transmission line elements replaced by Π section lumped-element equivalents.

prototype 10-V programmable Josephson voltage standard is also built and utilized as an on-chip power detector to evaluate the amplitude balance of the divider. Finally, the unit cell is successfully implemented in Triquint's commercial TQPED[1] process at room temperature with a modest penalty in area and loss.

II. Broadband Lumped Element CPW Wilkinson

A lumped-element Wilkinson power divider can be synthesized by replacing the typical physical $\lambda/4$ sections of transmission line with lumped-element equivalent Π networks [11]. This lumped-element topology allows a tenfold reduction in physical length. The availability of superconducting planar spiral inductors allows multiple lumped-element $\lambda/4$ equivalent sections in a broadband Butterworth configuration [5], [12]–[15]. The two-section Wilkinson power divider, shown in Fig. 2, incurs a negligible penalty in loss and a very modest 30% increase in area for approximately double the BW compared to that of a single-section lumped-element Wilkinson divider.

[1]Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experimental procedure adequately. Such identification is not intended to imply recommendation or endorsement by NIST, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

TABLE I
L_s and C_p Values for $\lambda/4$ Π Equivalent Sections of Various Useful Impedances at 20 GHz

Z_0	L_s	C_p	Comment
35 Ω	280 pH	230 fF	Branch line coupler Z_{BL}
42 Ω	335 pH	190 fF	Broadband Wilkinson Z_{01}
50 Ω	400 pH	160 fF	Balanced divider Z_0
60 Ω	475 pH	135 fF	Broadband Wilkinson Z_{02}
70 Ω	560 pH	110 fF	Standard Wilkinson Z_{Wilk}

A. Design

The values for a cannonical low-pass Π network with series inductance L_s and shunt capacitance C_p of electrical length θ in radians, frequency f_0 in hertz, and characteristic impedance Z_0 in ohms are given by [11]

$$L_s = \frac{\theta \cdot Z_0}{\pi^2 \cdot f_0} \text{ and } C_p = \frac{\theta}{\pi^2 \cdot f_0 \cdot Z_0}. \quad (1)$$

While used most often to realize $\lambda/4$ transmission-line segments, these expressions can be used to generate arbitrary length and impedance transmission-line equivalents. This allows pseudodistributed circuit design in lumped elements, examples of which are shown in Table I.

A broadband Wilkinson power divider can be synthesized by replacing the single $\lambda/4$ matching section from 100 to 50 Ω in the forward even-mode Wilkinson analysis circuit with multiple $\lambda/4$ sections designed for a Butterworth/binomial response. A published study of several possible distributed broadband Wilkinson designs shows that a design with two series (low-pass) $\lambda/4$ sections has a broader BW than a design with one series (low-pass) and one shunt (high-pass) $\lambda/4$ section, trading BW for out-of-band isolation [13]. A reduced component count and smaller area can be achieved by placing the additional series $\lambda/4$ section before, rather than after, the split between the two legs of the Wilkinson, as in Fig. 2(a), with negligible effect on divider performance.

Analysis of the even-mode half circuit, shown in Fig. 2(b), yields design equations for the characteristic impedance of each section Z_{01} and Z_{02} in terms of the desired input and output port impedances Z_{Port1} and Z_{Port2}, respectively,

$$2 \cdot Z_{01} = 2 \cdot Z_{\text{Port1}} \cdot e^{\left[2^{-2} \cdot K_0^2 \cdot \ln(Z_{\text{Port2}}/2 \cdot Z_{\text{Port1}})\right]} \quad (2)$$

$$Z_{02} = 2 \cdot Z_{01} \cdot e^{\left[2^{-2} \cdot K_1^2 \cdot \ln(Z_{\text{Port2}}/2 \cdot Z_{\text{Port1}})\right]}. \quad (3)$$

These expressions are derived from the general binomial transformer equations [14]

$$Z_{m+1} = Z_m \cdot e^{\left[2^{-M} \cdot K_n^M \cdot \ln(Z_{out}/Z_{in})\right]} \quad (4)$$

$$K_m^M = \frac{M!}{(M-m)! \cdot m!}. \quad (5)$$

Here, M is the total number of binomial transformer sections and m is the current section.

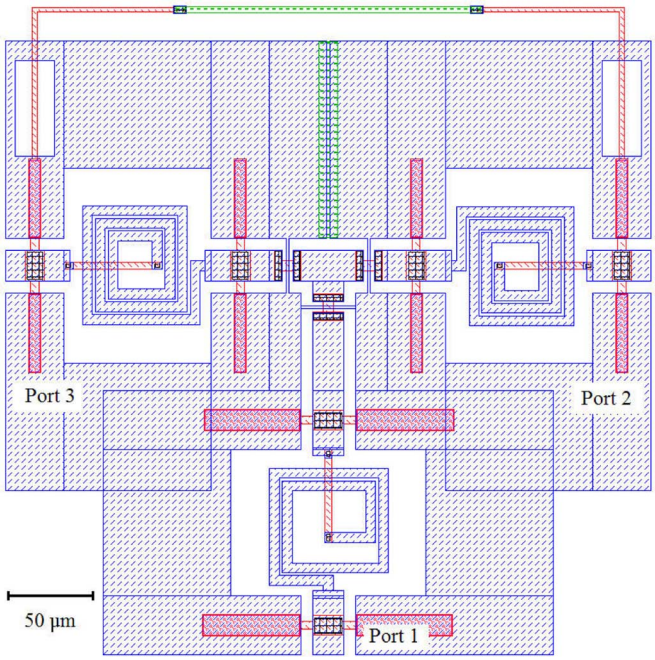

Fig. 3. Layout of the broadband lumped-element 20-GHz Wilkinson from Fig. 2(c). Red (in online version) ⧅ hatch is Nb1, black ⊞ hatch is Nb1–2 via, blue (in online version) ⧄ hatch is Nb2 and green (in online version) ⧈ hatch is AuPd. Solid blue lines (in online version) in the CPW ground planes show the HFSS simulation cell boundaries. Approximate divider dimensions are 400 μm $(0.07\lambda)\times$ 300 μm (0.05λ) with minimum trace width and spacing of 1.5 μm (0.0002λ).

These distributed sections can then be converted to *LC* Π $\lambda/4$ sections using (1), as shown in Fig. 2(c). For a two-stage broadband Wilkinson centered at 20 GHz, the desired $\lambda/4$ section impedances and corresponding *L* and *C* values are shown in Table I. These values are well within the range of impedance values realizable in the NIST IC process discussed in Section II-B.

The lumped-element Wilkinson models derived from the closed-form expressions were optimized in Agilent's ADS[1] circuit simulator to obtain the desired tradeoff between BW and reflections. Initial layout geometries were obtained based on an ideal parallel plate capacitor model and Stanford Spiralcalc [16] planar spiral inductor models, then simulated and tuned as single *L* and *C* elements embedded in a CPW transmission line using Ansoft's High Frequency Structure Simulator (HFSS) v10[1] 3-D FEM simulator. Superconducting Nb traces are modeled with 3-D perfect electric conductors (PECs) in HFSS. The solid blue lines (in the online version) in the ground planes of the divider layout in Fig. 3 indicate the HFSS cell boundaries.

The HFSS results were exported as S-parameter blocks into ADS for further tuning of the entire circuit via this hybrid simulation. This final design was then verified using a complete HFSS simulation. For comparison: the single *L* or *C* element HFSS simulations required less than 50 000 tetrahedra, a few hundred megabytes of memory, and less then 20 min of processor time per element simulation; the hybrid simulations in ADS utilized a few megabytes of memory and less than 1 min; the full divider simulations in HFSS required 141 000 tetrahedra, over 4 GB of memory space, and 7 h of real time to solve on a 32-bit Pentium D 3.4 GHz with 3-GB RAM.[1]

TABLE II
NIST IC FABRICATION PROCESS LAYER STACK. Nb TRACES ARE MODELED IN HFSS USING PEC. Nb1 AND Nb2 ARE USED WITH THE SiO_2 INTERLAYER DIELECTRIC TO FORM MIM CAPACITORS. THE JJ BARRIER IS NOT USED IN THE DIVIDER CIRCUITS

Layer name	Material	h [μm]	Properties
Resistor	AuPd	0.13	$\sigma = 4\,\mathrm{E}^6\,\mho/\mathrm{m}$
Nb2	Nb	0.70	∼PEC
MIM oxide	SiO_2	0.30	$\epsilon_r = 4.5$
JJ electrode	Nb	0.17	not used here
JJ barier	Nb_xSi_{1-x}	0.01	not used here
Nb1	Nb	0.30	∼PEC
Oxide	SiO_2	0.15	$\epsilon_r = 4.5$
Substrate	Si	380	$\epsilon_r = 11.5$

B. Layout and Fabrication

The NIST superconducting IC fabrication process layer stack is shown in Table II. Minimum linewidths and spacings are 1 μm for all layers. This process generates resistors of $\sim 2\,\Omega/\square$, metal–insulator–metal (MIM) capacitors of ~ 0.1 fF/μm^2, and under-passed spiral inductors in the range of 100–5000 pH. Lumped $\lambda/4$ sections with L_s and C_p integrated into Nb on Si CPW with a center conductor width of 16 μm and gap of 8 μm can be realized in a 130-μm length of CPW, as compared to 1600 μm for a distributed $\lambda/4$ section at 20 GHz.

Fig. 3 shows a typical layout of a 20-GHz center-frequency broadband lumped-element Wilkinson power divider with 50-Ω input and output impedances. Approximate dimensions of this lumped-element Wilkinson are 400 μm $(0.07\lambda)\times$ 300 μm (0.05λ), as compared with a standard distributed Wilkinson at 20 GHz, which would be approximately 1600 μm $(0.25\lambda)\times 400$ μm (0.07λ) in this technology.

Several test circuits were considered to facilitate testing, shown in Fig. 4. In the test circuit 1, Fig. 4(a), no on-chip termination is required, but the port 2 and port 3 S-parameter responses are not directly measurable. In addition, power reflections between the two dividers can cause deviations in the measurement from the desired matched load case. Circuit 2 [see Fig. 4(b)] allows port 2 characterization, but introduces another unknown in the on-chip termination. Circuit 3 [see Fig. 4(c)] uses an on-chip resistive termination at port 1. This allows isolation characterization of port 2 to port 3 with the caveat of a separate physical device and possible process variations across the wafer. Only circuits 2 and 3 were realized for Wilkinson unit-cell testing. All superconducting circuits reported here were fabricated in the NIST Boulder Quantum Device Fabrication Facility.

C. Testing

Measurements were performed with an Agilent 8722ES[1] vector network analyzer (VNA). Calibration was accomplished using on-chip through-reflect (short)-line (1.5 mm) (TRL) standards custom-fabricated with a band of 8–35 GHz at 4K immersed in a liquid helium $(\epsilon_r = 1.005)$ dewar. The repeatability of the measurements is limited by several factors in the test setup. The calibration procedure requires three thermal cycles from room temperature to 4 K, boiling $\sim$ 1 L of helium.

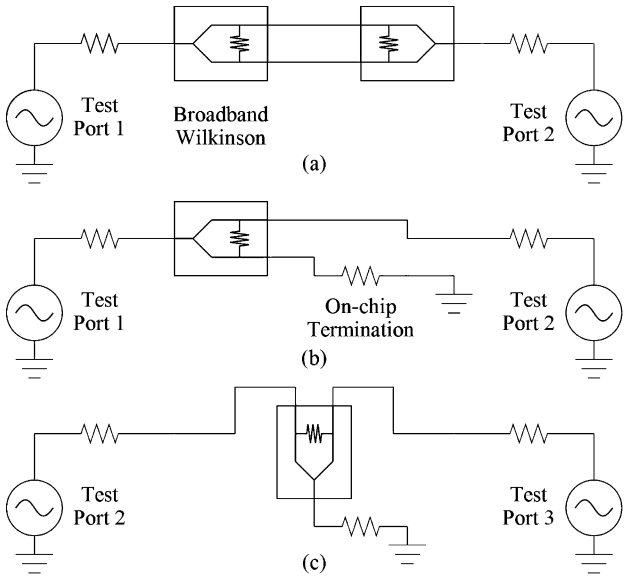

Fig. 4. Three-port Wilkinson divider to two-port network analysis conversion circuits. (a) Circuit 1: back-to-back dividers. (b) Circuit 2: port 3 terminated on-chip. (c) Circuit 3: port 1 terminated on-chip.

TABLE III
BROADBAND DIVIDER MEASUREMENT SUMMARY COMPARING THE NIST SUPERCONDUCTING IC PROCESS, SECTION II, AND THE TRIQUINT COMMERCIAL TQPED PROCESS[1], SECTION IV. SUMMARY DATA IS CALCULATED FROM THE RESULTS SHOWN IN FIGS. 5, 6, AND 11

Process	Parameter	$BW\|_{-10\,\mathrm{dB}}$	Ave$\|_{15\ \mathrm{GHz}}^{22\ \mathrm{GHz}}$	Max$\|_{15\ \mathrm{GHz}}^{22\ \mathrm{GHz}}$
NIST	S_{11}	10–25 GHz	–21.7 dB	–17.4 dB
NIST	S_{22}	10–25 GHz	–16.6 dB	–12.9 dB
NIST	S_{23}	13–30 GHz	–15.6 dB	–13.3 dB
NIST	S_{33}	10–28 GHz	–19.9 dB	–16.6 dB
NIST	IL	–	0.1 dB	0.4 dB
TQPED	S_{11}	10–25 GHz	–23.0 dB	–19.2 dB
TQPED	S_{22}	10–24 GHz	–23.3 dB	–18.0 dB
TQPED	IL	–	0.6 dB	0.9 dB

This changes the thermal gradient along the 1.2-m cryoprobe coaxial cable; hence, its electrical length and loss, with each successive measurement. The chip contact is made via a pressure screw that engages a set of copper–beryllium (Cu–Be) spring fingers with the gold–palladium (Au–Pd) coated pads on the chip with only moderate repeatability. The economical subminiature A (SMA) connectors used have resonances in the upper end of the band of interest. A flip-chip bonded permanent mounting solution has been developed by the authors to address these issues in the final programmable Josephson voltage standard system [17], but is not practical for use with the many test circuits and VNA calibration standards needed here.

Table III shows a summary of Wilkinson divider test circuit measurement results. Fig. 5 shows a comparison of HFSS simulations and measurements for test circuit 2 from Fig. 4(b). HFSS simulation and measurement results for test circuit 3 from Fig. 4(c) are shown in Fig. 6. The 15–22-GHz band is considered the band of interest for this design, allowing for ample tuning around the 20-GHz junction array design point. Average

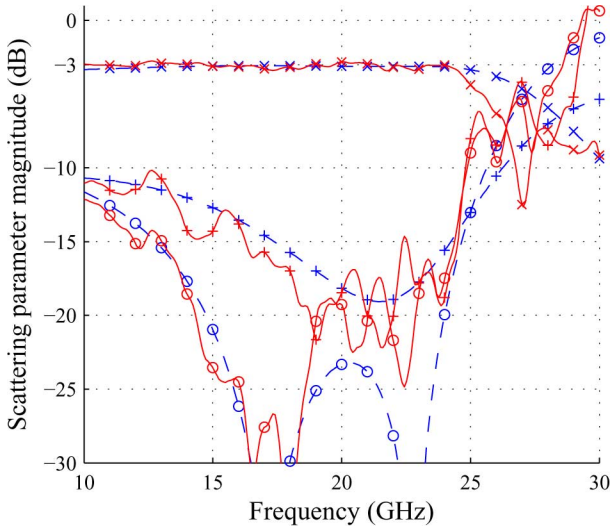

Fig. 5. Broadband lumped-element Wilkinson (Fig. 3) HFSS simulated data (blue dashed lines in online version) and measurement results (red solid lines in online version) from test circuit 2 [see Fig. 4(b)] using 4K TRL calibration on-chip. S_{11} is marked with $\circ$, S_{21} with $\times$, and S_{22} with $+$.

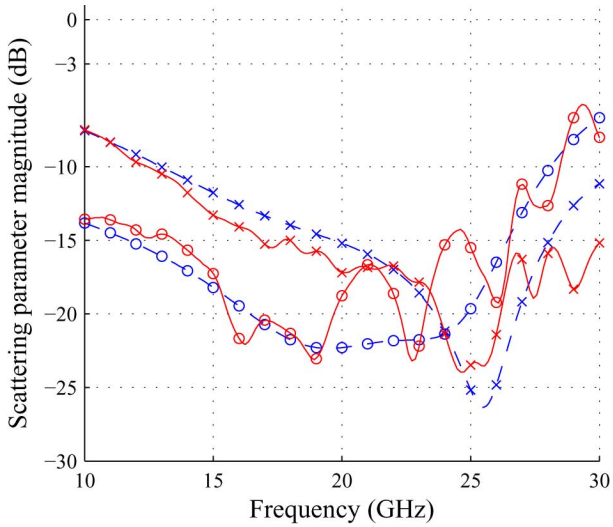

Fig. 6. Broadband lumped-element Wilkinson (Fig. 3) HFSS simulated data (blue dashed lines in online version) and measurement results (red solid lines in online version) from test circuit 3 [see Fig. 4(c)] using 4K TRL calibration on-chip, in red solid lines (in online version). S_{23} is marked with $\times$, S_{33} is marked with $\circ$.

in-band values in Table III are computed as the base-10 logarithm of mean power

$$\mathrm{Ave}|S_{ij}| = 10 \cdot \log_{10}\left[\mathrm{Mean}|_{15\ \mathrm{GHz}}^{25\ \mathrm{GHz}}(|S_{ij}|)^2\right]. \tag{6}$$

Insertion loss (IL) for this work is defined as

$$\mathrm{IL} = -10 \cdot \log_{10} \frac{\sum_{i=2}^{N}\left(|S_{i1}|^2\right)}{1-|S_{11}|^2}. \tag{7}$$

By circuit symmetry and from simulation results, S_{31} is assumed to be approximately equal to S_{21} for IL calculations in Table III.

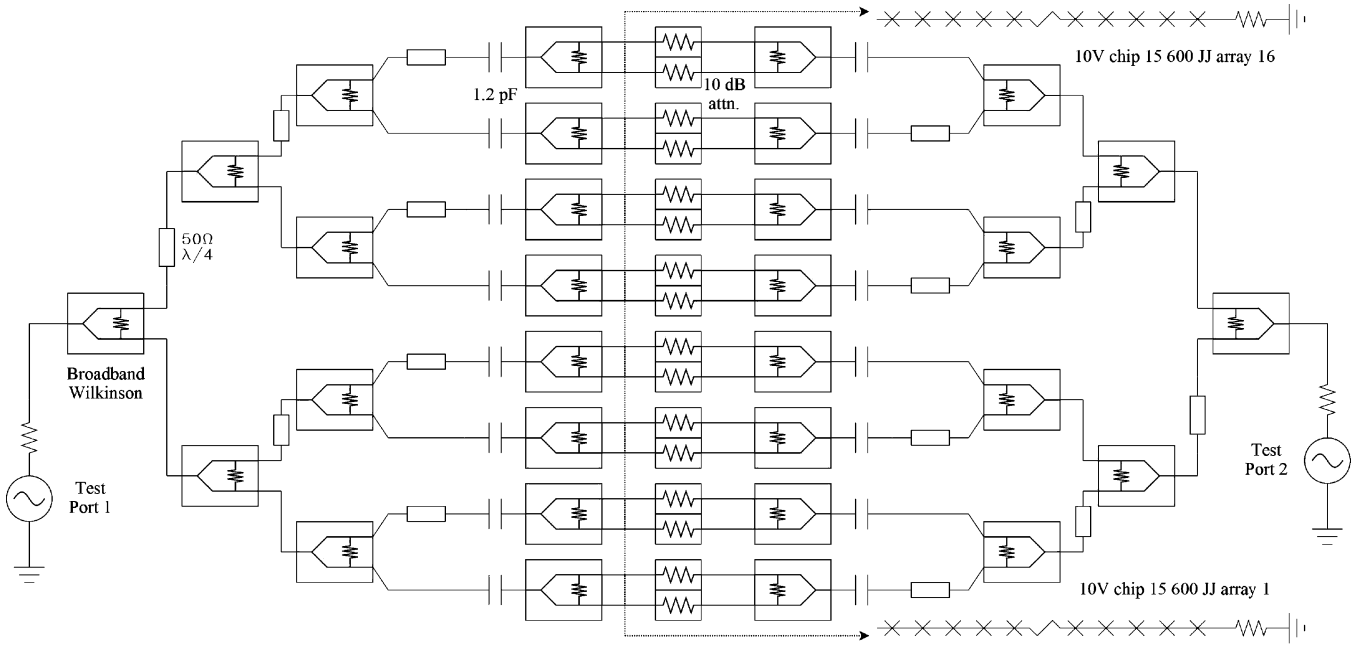

Fig. 7. Simplified schematic of the balanced divider/attenuator/combiner configuration test circuit, showing broadband lumped-element Wilkinson power dividers, $\lambda/4$ lumped Π sections for reflection cancellation, 10-dB isolation attenuators, and 1.2-pF coupling capacitors between the third and fourth levels of division and combination. Simulated transmission line interconnects and bends are not shown. The dotted cut plane indicates the position of the junction arrays in the 10-V programmable Josephson voltage standard.

III. Balanced 16-Way Power Divider

The concept of a balanced divider/combiner (D/C), widely used in broadband amplifier design [14], can be applied here to achieve a many-way power division to many identical arrays of junctions. A balanced divider relies upon the fact that each array has a nearly identical return loss. By inserting an additional $\lambda/4$ transmission line between port 2 of the Wilkinson and the junction array, the round-trip reflection path is 180° longer than the corresponding round-trip reflection path from the junction array connected to port 3 of the Wilkinson. These two reflections are out of phase at port 1 and cancel, leading to a well matched and very broadband system. Many-way power division can be achieved as shown in Fig. 7. This solution addresses the fundamental issue with 360°, round-trip in-phase reflection combining in N-way even-$\lambda/4$-section binary power dividers reported in [6]. Here, the total interconnect layout length between dividers is unconstrained, only the $\lambda/4$ delta between branches (implemented in lumped elements) is required.

A. Design

A 16-way power split allows 16 junction arrays of 15 600 junctions [2] fabricated on a prototype 10-V programmable Josephson voltage standard chip at 20 GHz reported in [3]. The chip area required for a 16-way divider on-chip is reduced by a factor of 4 using the lumped-element Wilkinson dividers and $\lambda/4$ 50-Ω *LC* Π sections, from Table I, compared to the previously used single $\lambda/4$ distributed matching sections. The entire 16-way divider network is simulated in ADS using the hybrid simulation methodology discussed in Section II-A.

In order to appropriately characterize a many-way divider, a test circuit is needed that preserves both the desired loading at the output, as well as the ability to measure IL through the device. The back-to-back circuit shown in Fig. 4(a) has a fundamental flaw of terminating a divider circuit with its own complex output impedance, rather than the desired real 50-Ω load needed to obtain valid S-parameters. To solve this problem 10-dB attenuators are monolithically integrated between the divider circuit under test, and the combiner output circuit. A schematic of this balanced divider/attenuator/combiner (D/A/C) configuration is shown in Fig. 7.

Identical length 50-Ω CPW superconducting transmission lines were used to interconnect the divider, attenuators, and combiner; the $\lambda/4$ sections were arranged such that the net phase delays along any given division and recombination path are equal. A 1.2-pF coupling capacitor was inserted between the third and fourth levels of power division and recombination to ac-couple each pair of junction arrays and enable connecting all of the arrays in series at dc to achieve 10 V. A lithographically identical 10-dB attenuator was fabricated on the same test chip as the D/A/C to allow deembedding of the divider performance.

B. Testing

The 16-way D/A/C configuration test chip was evaluated in the same manner as the Wilkinson divider chips, discussed in Section II-C. A 16-way D/C test circuit without attenuators, shown in Fig. 1, was also fabricated and tested to demonstrate the utility of the added attenuators. Figs. 8 and 9 compare measured and simulated results from the 16-way balanced D/C and D/A/C configurations, respectively. Table IV summarizes the measurement data from both configurations and the 10-dB attenuator (10 dB A). The measured IL and return loss of the back-to-back test configuration both improve markedly with the

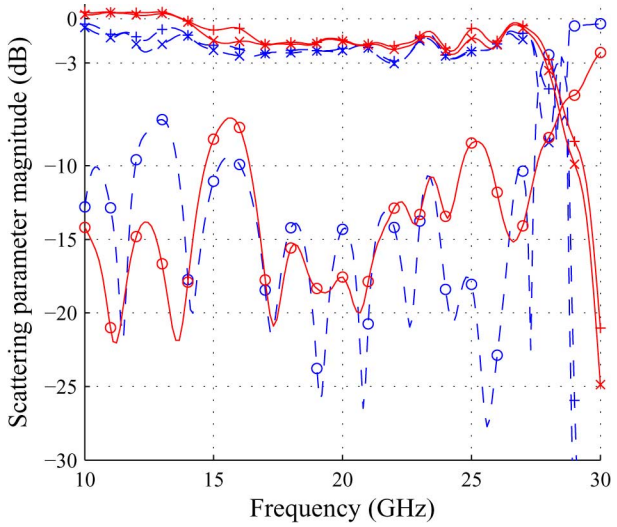

Fig. 8. D/C configuration measured versus simulated results for 16-way balanced broadband Wilkinson divider (Fig. 1). Hybrid HFSS 3-D FEM and ADS circuit simulated data (blue dashed lines in online version), and measurements using 4K TRL calibration on-chip (red solid lines in online version). S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and IL is marked with $+$. Note the standing waves between the divider and the combiner apparent in the S_{11} measurement.

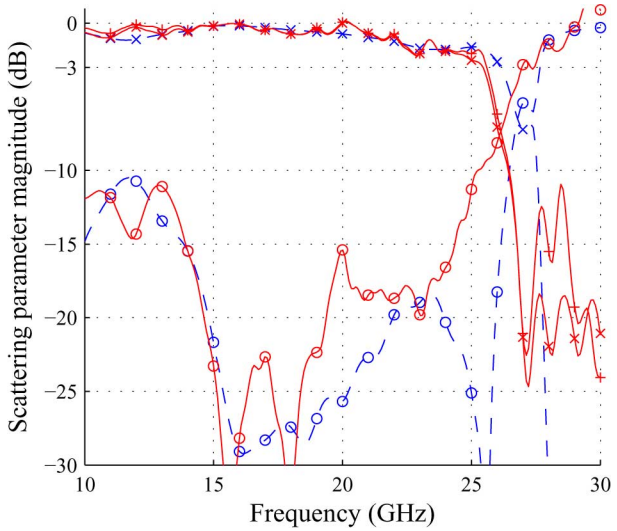

Fig. 9. D/A/C configuration 16-way balanced Wilkinson divider measured versus simulated (Fig. 7) results. S_{21} and IL are calculated by deembedding the 10-dB attenuator data from the D/A/C test configuration data. Hybrid HFSS 3-D FEM and ADS circuit simulated data (blue dashed lines in online version), and measurements (red solid lines in online version) using 4K TRL calibration on-chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and IL is marked with $+$.

incorporation of the 10-dB attenuators. This D/A/C configuration is a useful measurement technique for characterization of many-port integrated dividers.

Assuming the loss in the division is the same as the loss in the recombination, the average and maximum IL through a single 16-way divider network $\mathrm{IL}_{\mathrm{divider}}$ can be computed as half of the total for the D/C, $\mathrm{IL}_{\mathrm{total}}$. The D/A/C measured data in Fig. 9 and Table IV has been calculated by deembedding the measured IL of a matched lithographically identical 10-dB attenuator on the same chip. The 0.5-dB maximum 16-way power divider loss is very small compared to the 3-dB cable loss incurred in the

TABLE IV
16-WAY BALANCED DIVIDER SUMMARY. VALUES ARE CALCULATED FROM THE MEASUREMENTS OF D/C CONFIGURATION (FIG. 8), THE ON-CHIP 10-dB ATTENUATOR, AND D/A/C CONFIGURATION (FIG. 9)

Config.	Parameter	$BW\|_{-10\,\mathrm{dB}}$	Ave$\|^{22\,\mathrm{GHz}}_{15\,\mathrm{GHz}}$	Max$\|^{22\,\mathrm{GHz}}_{15\,\mathrm{GHz}}$
D/C	S_{11}	16.5-24.5 GHz	–11.6 dB	–6.7 dB
D/C	IL_{total}	–	1.4 dB	2.2 dB
D/C	IL_{divider}	–	0.7 dB	1.1 dB
D/A/C	S_{11}	10-25 GHz	–20.5 dB	–15.1 dB
D/A/C	IL_{total}	–	10.0 dB	10.5 dB
10 dB A	S_{11}	10-30 GHz	–25.7 dB	–21.4 dB
10 dB A	IL	–	9.5 dB	9.9 dB
D/A/C	IL_{divider}	–	0.2 dB	0.5 dB

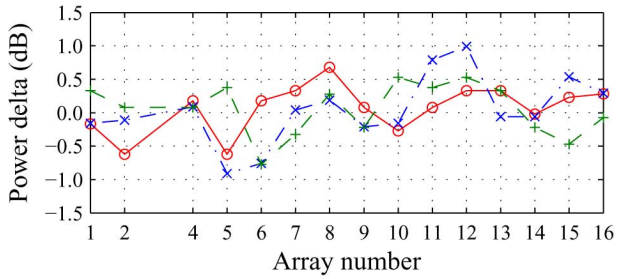

Fig. 10. Measured power division uniformity results from broadband Wilkinson in 16-way balanced divider feeding a prototype 10-V chip with 16 arrays of 15 600 junctions at 15 GHz (red solid line in online version marked $\circ$), 19 GHz (blue dashed–dotted line in online version marked $\times$), and 22 GHz (green dashed line in online version marked $+$). The x-axis indicates the array number, coinciding with Fig. 7 with 1 at the bottom and 16 at the top. The y-axis is the change from nominal source input power at which each array exhibits a equal I_{bias}/I_C ratio (an indicator of equal microwave power delivered to that array).

1.2-m cryoprobe, or to any commercially available broadband divider solution in the 15–22-GHz band. While not measured, the simulated isolation of the 16-way divider is similar for adjacent branches, and improved for nonadjacent branches, when compared to the single Wilkinson divider.

The bulk of the IL is due to the balanced out-of-phase divider reflections producing a voltage drop across the Wilkinson isolation resistor before they cancel. This assertion is supported by simulations, as well as the noted drop in IL with the addition of the attenuators, suppressing the reflections from the combiner. A tradeoff in a balanced divider, versus a standard corporate divider without the $\lambda/4$ reflection canceling sections, is that the uniformity of division in simulations suffers slightly away from the center frequency of the $\lambda/4$ section. By inspection, a balanced divider will have a 90° phase progression between outputs rather than phase balance.

A prototype 10-V programmable Josephson voltage standard was fabricated using the 16-way balanced divider to split a single microwave feed from a room temperature power amplifier into 16 arrays of 15 600 junctions each [3]. The dc-bias current range over which the Shapiro zero-voltage step is quantized in the junction dc *IV* curve is a strong indicator of microwave current through the junction [2]. This property allows the arrays themselves to be used as an on-chip relative power meter to evaluate the amplitude balance of the divider. Fig. 10 shows the amplitude balance of the divider at 15, 19,

TABLE V
COMPARISON OF **THIS WORK** AND OTHER PUBLISHED AND COMMERCIALLY AVAILABLE POWER DIVIDERS SORTED BY N, THEN IL/BW

N	f_-[GHz]	f_+[GHz]	BW[%]	IL[dB]	S_{11}[dB]	Topology	Size [mm × mm × mm]	Reference
16	**15.0**	**22.0**	**37.8**	**0.5**	**-15.0**	**Lumped Nb on Si, Fig. 7**	**4.9 x 1.5 x 0.4**	**Fig. 9, 15–22 GHz**
16	**13.0**	**25.0**	**63.2**	**1.1**	**-10.0**	**Lumped Nb on Si, Fig. 7**	**4.9 x 1.5 x 0.4**	**Fig. 9, Full band**
16	10.0	10.8	6.7	0.3	-15.5	Radial cavity to SMA	∼500 x ∼500 x ∼20	Ciao 100107-1601[1]
16	10.2	12.0	16.2	2.5	-15.0	Substrate integrated WG	200 x 120 x 0.5	Z.C. Hao [7]
8	4.0	18.0	127.3	1.2	-11.7	Stripline to SMA	63 x 108 x 10	Empower 0400-0151[1]
8	8.0	18.0	76.9	2.0	-12.7	Stripline to SMA	61 x 101 x 10	ATM P816H[1]
8	2.5	8.5	109.1	∼2.5	-12.7	Microstrip to SMA	64 x 16 x 0.3	J. Zhou [6]
8	0.5	18.0	188.2	6.5	-11.7	Stripline to SMA	161 x 152 x 13	Narda 4426-8[1]
4	6.0	18.0	∼100.0	0.8	-12.0	MS on alumina	40 x 20 x 16	A.R. Barnes [8]
4	22.0	26.0	16.7	2.4	-15.5	Lumped 0.13 um CMOS	0.33 x 0.33 x .3	J.G. Kim [9]
2	**13.0**	**24.0**	**61.3**	**0.4**	**-10.0**	**Lumped Nb on Si, Fig. 3**	**0.3 x 0.4 x 0.4**	**Fig. 5, Full band**
2	4.0	12.0	100.0	∼0.6	∼-10.0	180° Parisi Hybrid Nb on Si	1.4 x 0.5 x 0.4	A.R. Kerr [5]
2	**15.0**	**22.0**	**37.8**	**0.9**	**-18.0**	**Lumped Au on GaAs, Fig. 2 (c)**	**1.2 x 1.5 x 0.1**	**Fig. 11, 15–22 GHz**
2	**10.0**	**24.0**	**82.4**	**1.4**	**-10.0**	**Lumped Au on GaAs, Fig. 2 (c)**	**1.2 x 1.5 x 0.1**	**Fig. 11, Full Band**
2	17.5	22.5	25.0	0.6	-15.0	Ti/Au on micromachined Si	0.3 x 0.4 x 0.3	L.H. Lu [10]
2	22.0	26.0	16.7	1.4	-8.9	Lumped 0.13 um CMOS	0.12 x 0.29 x 0.3	J.G. Kim [9]

and 22 GHz across the 16 output arrays. This data is derived from a measurement of $I_{\rm bias}/I_C$ for the top of the zero-voltage Shapiro step over a sweep of power from approximately 2 to 200 mW on-chip for all 16 arrays. The normalization by I_C helps account for junction variation across the wafer, where I_C is the junction critical current [1]. With the exception of array 3, all of the arrays cross an arbitrarily selected constant $I_{\rm bias}/I_C$ within a ±1-dB range of input power, indicating a good microwave power division amplitude balance. Array three displayed an isolated junction fabrication defect and is omitted.

IV. DISCUSSION AND CONCLUSIONS

Table V shows a comparison of this work to other published and commercially available N-way power dividers. Comparisons can be made upon the basis of number of divider outputs, N, BW (defined by match and isolation specification S_{11}), BW, maximum IL in band, IL, and size. Table V is sorted first by N, then by IL/BW to aid in this comparison. The availability of superconducting low-loss inductors enables very large and complex circuits including many $\lambda/4$ lumped Π sections to emulate distributed microwave circuit designs in a small fraction of the area with very little penalty in loss. This work exhibits the best BW and IL for its size scale, normalized across N, when compared to published work and commercially available devices.

The lumped-element Wilkinson divider shown in Fig. 2(c) was also implemented in the Triquint commercial TQPED[1] GaAs monolithic microwave integrated circuit (MMIC) process in 4-μm-thick gold microstrip on a 100-μm substrate. The port 1 and port 2 through test configuration shown in Fig. 4(b) was designed and fabricated requiring an area of approximately 1200 μm× 1500 μm. This normal metal design at room temperature exhibited a measured average IL of 0.6 dB compared to the measured superconducting device average IL of 0.1 dB in the 15–22-GHz band of interest, shown in Table III. The measured and simulated S-parameters of this device are compared

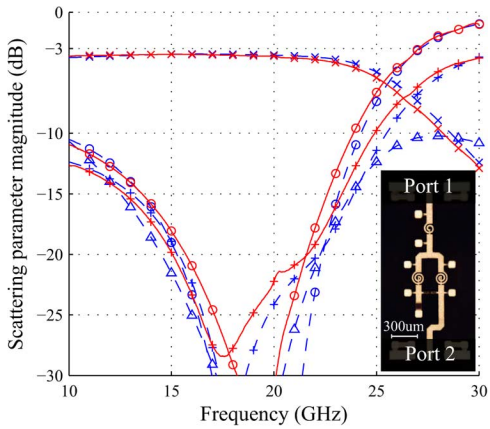

Fig. 11. Broadband lumped-element TQPED Wilkinson simulated data (blue dashed lines in online version) and measurement results (red solid lines in online version) using room-temperature TRL calibration on-chip. S_{11} is marked with ∘, S_{21} is marked with ×, and S_{22} is marked with +. This device was fabricated using the commercial Triquint TQPED[1] GaAs MMIC process and tested at room-temperature. Port 3 is terminated with an on-chip resistor. The inset is a micrograph of the fabricated device.

in Fig. 11 using wafer probe measurements with on-chip TRL calibration. Even without the advantage of superconducting inductors, this implementation compares favorably to other published and commercial dividers, as shown in Table V. This validates the broadband lumped-element design methodology presented here for room-temperature IC design with a modest penalty in loss and area.

In this work, very broadband low-loss compact lumped-element many-way Wilkinson power dividers were demonstrated using NIST and Triquint TQPED[1] microfabrication processes. A balanced power division solution was presented to address the fundamental in-phase reflections problem of an even-$\lambda/4$-segment many-way binary power divider [6]. This solution occupies less area than three-$\lambda/4$-segment dividers, and removes the

constraints on the interconnect layout, at the cost of phase balance. Additionally the balanced divider solution improves the divider match assuming phase and amplitude matched loads, as is often the case for integrated devices. A back-to-back test configuration for many-way dividers utilizing integrated 10-dB attenuators was devised to present a 50-Ω load at the divider output while maintaining the ability to measure IL through the device. The area and performance gains of these innovative circuits over conventional distributed power dividers are an enabling microwave technology for the NIST 10-V programmable Josephson voltage standard.

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