Circuit Simulation Model for a 100 A, 10 kV Half-Bridge SiC MOSFET/JBS Power Module

T. H. Duong, A. Rivera-López, A. R. Hefner, Jr. , and J. M. Ortiz-Rodríguez

National Institute of Standards and Technology
Semiconductor Electronics Division
Gaithersburg, MD 20899

Abstract- **This paper presents the simulation of a 100 A, 10 kV Silicon Carbide (SiC) half-bridge power module operating at 20 kHz in a behavioral boost converter circuit. In the half-bridge power module, 10 kV SiC power MOSFETs are used as the upper and lower switches, where 10 kV SiC Junction Barrier Schottky (JBS) anti-parallel diodes along with 100 V silicon JBS series reverse-blocking diodes are used to protect the SiC MOSFETs from reverse conduction. The behavioral boost converter is designed to operate a single power switch and a single power diode for continuous 20 kHz hard switching conditions at 5 kV and 100 A. The test circuit contains the model for the 100 A, 10 kV SiC half-bridge power module where the upper MOSFET gate is turned off. The simulated waveforms demonstrate fast switch performance (<100 ns) with minimal turn-on current spikes resulting from charging the capacitances of the other MOSFET and JBS diodes in the module. The results also indicate that the combination of the 10 kV SiC JBS anti-parallel diode with the series low-voltage silicon JBS reverse-blocking diode is effective in protecting the SiC MOSFETs from reverse conduction.**

I. INTRODUCTION

Recent breakthroughs in Silicon Carbide (SiC) material and fabrication technology have led to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability [1]. With the emergence of this new SiC device technology, various industry and government programs have been established to investigate future high-voltage power conversion systems enabled by these devices [2]. The goal of the DARPA WBGS-HPE Phase II program is to develop 100 A, 10 kV SiC power modules required to demonstrate a 2.7 MVA Solid State Power Substation (SSPS) in DARPA WBGS-HPE Phase III [2]. The purpose of this paper is to present a circuit simulation model for the 100 A, 10 kV SiC half-bridge power module including the recently developed 10 A, 10 kV SiC power MOSFETs and Junction Barrier Schottky (JBS) diodes [3]. This half-bridge power module model will be used to perform the simulations necessary to design the SSPS in DARPA WBGS-HPE Phase III.

The 100 A, 10 kV SiC half-bridge power module model developed in this paper includes the recently developed model for the 10 kV SiC power MOSFET [4] and a new model developed in this paper for the 10 kV SiC JBS diode. The single die MOSFET and JBS diode models are area scaled and paralleled to produce the 100 A module current ratings. The multi-chip area scaling method is validated by using parameter extraction and comparison with experiments for two different die sizes (5 A and 10 A) and for modules with paralleled die. Simulations are performed using the 100 A, 10 kV module model in a previously developed boost converter test circuit [5] in order to demonstrate the module model performance. Simulation results indicate that the combination of the anti-parallel 10 kV JBS diode with the series low-voltage silicon diode is effective in protecting the SiC MOSFETs from reverse conduction.

II. MODEL DEVELOPMENT AND VALIDATION

Fig. 1 shows the schematic of the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module. Because SiC power MOSFETs can not be safely operated with reverse current conduction through the internal MOSFET body diode [6], the module includes an anti-parallel diode and a reverse-blocking series diode for both the upper and lower SiC MOSFET switches in the module. A 10 kV SiC JBS diode is used for the anti-parallel diode and a low-voltage (< 100 V) Si JBS diode is used for the series blocking diode. The series blocking diode is required because the high-temperature on-state voltage of the SiC JBS diode can exceed the 3 V required to turn on the internal body diode of the SiC MOSFET unless a very large area SiC JBS diode were used. Due to the drain-source junction capacitance of the SiC MOSFET, the series blocking Si JBS power diode needs to have high avalanche capability to prevent it from failure due to avalanche breakdown.

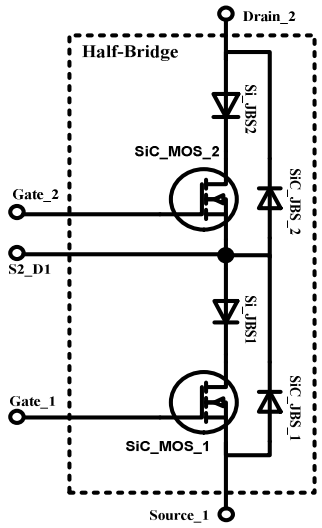


Fig. 1: Schematic of the 100 A, 10 kV half-bridge SiC MOSFET/JBS power module with series silicon JBS power diodes to prevent reverse conduction through the MOSFETs.

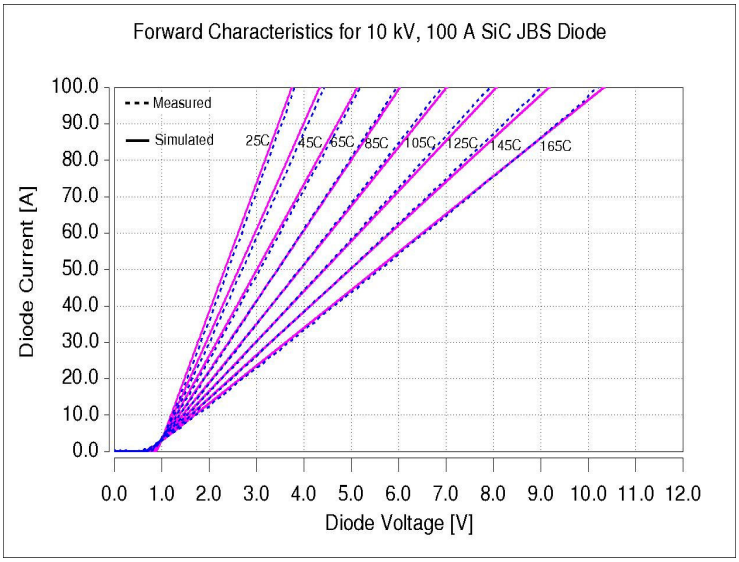


Fig. 2: Comparison of scaled measured (dashed) and simulated (solid) forward conduction characteristics at 25 °C, 45 °C, 65 °C, 85 °C, 105 °C, 125 °C, 145 °C, and 165 °C for a 100 A, 10 kV SiC JBS diode.

The 100 A, 10 kV SiC power MOSFET model is developed by area scaling the validated model presented in [4]. The model parameter extraction and validation for the 10 kV SiC JBS diode is performed for the first time in this paper. The scaling procedure is validated for the MOSFETs and JBS diodes using two different die sizes (5 A and 10 A) and 20 A and 100 A modules made by paralleling multiple die. As an example, Figs. 2 and 3 show the 100 A JBS diode model predictions compared with measured results area scaled to 100 A for both temperature dependence of on-state characteristics and dI/dt dependence of the reverse recovery current.

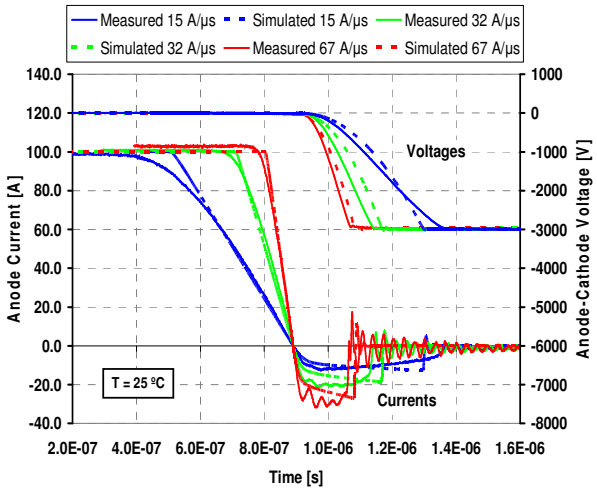
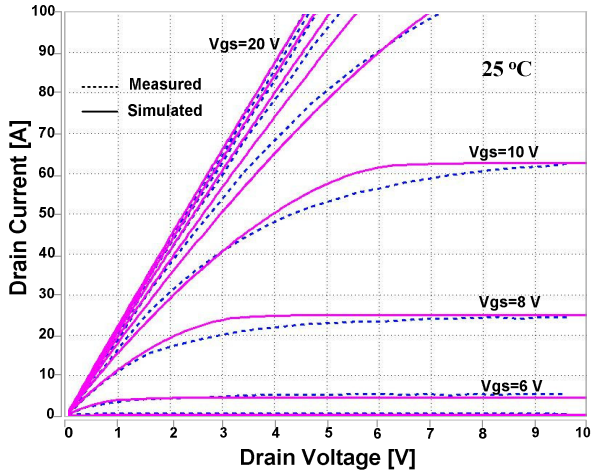


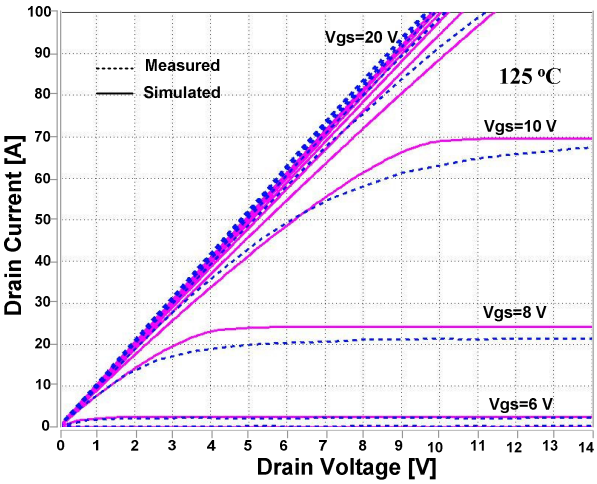
Fig. 3: Comparison of scaled measured (solid) and simulated (dashed) reverse recovery at 25 °C for a 100 A, 10 kV SiC JBS diode.

Fig. 4 shows the simulated (solid) model predictions compared with measured (dashed) results scaled to 100 A of output characteristics for a 10 kV SiC power MOSFET. These results are for temperatures of (a) 25 °C and (b) 125 °C. The curves are linear in the on-state region and have a pronounced change in curvature as the saturation or pinch-off region is approached. This occurs because the device has a large epitaxial layer resistance in series with the MOSFET channel, and the channel has a high transconductance. At 125 °C, there is less of a reduction in on-state resistance with temperature than for Si. This occurs because the effective channel mobility does not decrease with temperature for SiC as it does in Si. In the SiC MOSFETs, the channel mobility actually increases with temperature as more interface traps become occupied with the larger concentration of electrons available for conduction. The bulk mobility decreases with temperature in both SiC and Si as the temperature increases from 25 °C to 125 °C due to increased carrier scattering [7]. The resulting effect for SiC is a decrease in channel resistance that compensates for the increase in the drift layer series resistance.

Fig. 5 shows simulated model predictions (solid) compared with area scaled measured results (dashed) for a clamped inductive load turn-off with two different inductor current levels (80 A and 160 A) and a clamp voltage of 5 kV. The comparisons are for a 10 kV SiC power MOSFET area scaled to 100 A. The respective turn-off times are 50 ns for the 160 A case and 100 ns for the 80 A case.



(a)



(b)

Fig. 4: Comparison of scaled measured (dashed) and simulated (solid) output characteristics at 25 °C (a) and at 125 °C (b) for a 100 A, 10 kV SiC power MOSFET.

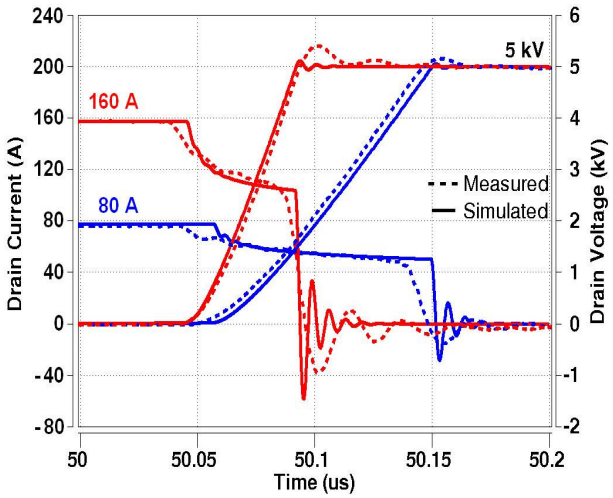


Fig. 5: Comparison of scaled measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms at 25 °C for a clamp voltage of 5 kV and a 100 A, 10 kV SiC power MOSFET.

III. Circuit Simulation Results

The schematic of the high-voltage behavioral boost converter test circuit is shown in Fig. 6 indicating the connection of the 10 kV, 100 A half-bridge power module, where the upper MOSFET gate is turned off with the gate resistor connected to – 5 V referenced to the source. The behavioral boost converter is designed to operate a single power switch and a single power diode for continuous 20 kHz hard switching conditions at 5 kV and 100 A. Measured results for a 5 A version of this circuit were presented in [5] to demonstrate the long-term switching performance of 5 kV, 5 A SiC power MOSFETs. This circuit is used to emulate the conditions of a hard-switching full-bridge converter including the capacitance of the upper and lower MOSFET and JBS diodes within the module. For this test circuit of Fig. 6, the upper MOSFET and the lower JBS diode of Fig. 1 are inactive similarly to on-half cycle of the full bridge converter.

As an example, Fig. 7 shows the simulated current and voltage waveforms of the active SiC MOSFET (SiC_MOS_1) and JBS diode (SiC_JBS_2) and capacitive current and voltage waveforms of the inactive components (SiC_MOS_2 and SiC_JBS_1) for turn-on and turn-off at 25 °C (solid) and 125 °C (dashed). The simulated waveforms demonstrate the gate resistor selection of 0.5 Ω results in fast switch performance (<100 ns) with minimal turn-on current spikes resulting from charging the capacitances of the other MOSFET and JBS diode in the module. The simulations also indicate that the combination of the 10 kV JBS anti-parallel diode with the series low-voltage silicon JBS reverse-blocking diode is effective in protecting the SiC MOSFETs from reverse conduction.

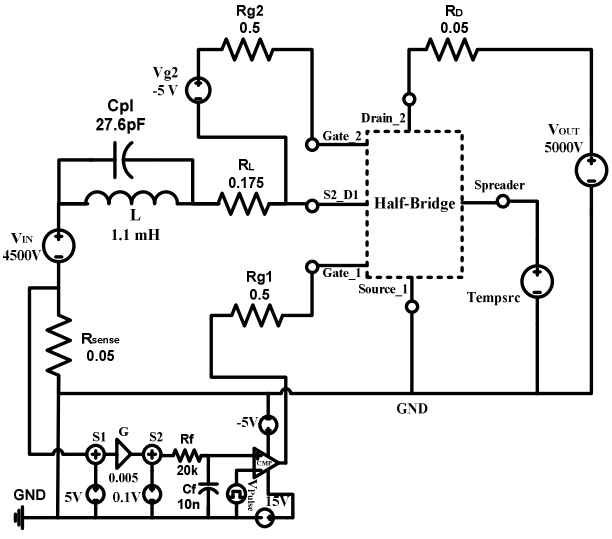


Fig. 6: Test circuit for evaluation of the 100 A, 10 kV SiC MOSFET/JBS power module model.

The waveforms of Fig. 7 are strongly influenced by the interaction of the conduction characteristics of the active devices with the capacitance-voltage characteristics of the other active and inactive devices in the module. The turn-on current waveform of the lower MOSFET has a steeper slope and larger overshoot at 125 ^{o}C than at 25 ^{o}C because the transconductance of the MOSFET increases with temperature [4]. In general, the MOSFET and diode junction capacitances decrease with increasing voltage across the devices resulting in current waveforms that change with voltage. For instance, during the lower MOSFET turn-on, the capacitive currents in the upper devices decrease with time as the voltage across these devices is increased. Conversely, the capacitive current in the lower JBS diode increases with time as the voltage across this diode is decreased during the lower MOSFET turn-on. Furthermore, the nonlinear gate-drain capacitance of the upper inactive MOSFET and the gate resistor of 0.5 Ω results in a gate voltage spike on the upper MOSFET of 0.6 V at 25 ºC and 1.3 V at 125 ºC during the turn-on of the lower MOSFET.

IV. CONCLUSION

A circuit simulation model was developed for a 100 A, 10 kV SiC half-bridge power module being developed by the DARPA WBGS-HPE Phase II program. The module contains 10-kV SiC power MOSFETs as the upper and lower switches, and 10 kV SiC JBS anti-parallel diodes along with 100 V silicon JBS series reverse-blocking diodes to prevent reverse conduction in the SiC MOSFET. A behavioral boost converter test circuit is used to evaluate the performance of the model and the module topology. The simulated waveforms demonstrate the selection of suitable gate resistors resulting in fast switch performance (<100 ns) with minimal turn-on current spikes. The simulations also demonstrate that the module topology is effective in protecting the MOSFET from reverse conduction. This half-bridge power module model will be used to perform simulations necessary to design the SSPS in DARPA WBGS-HPE Phase III.

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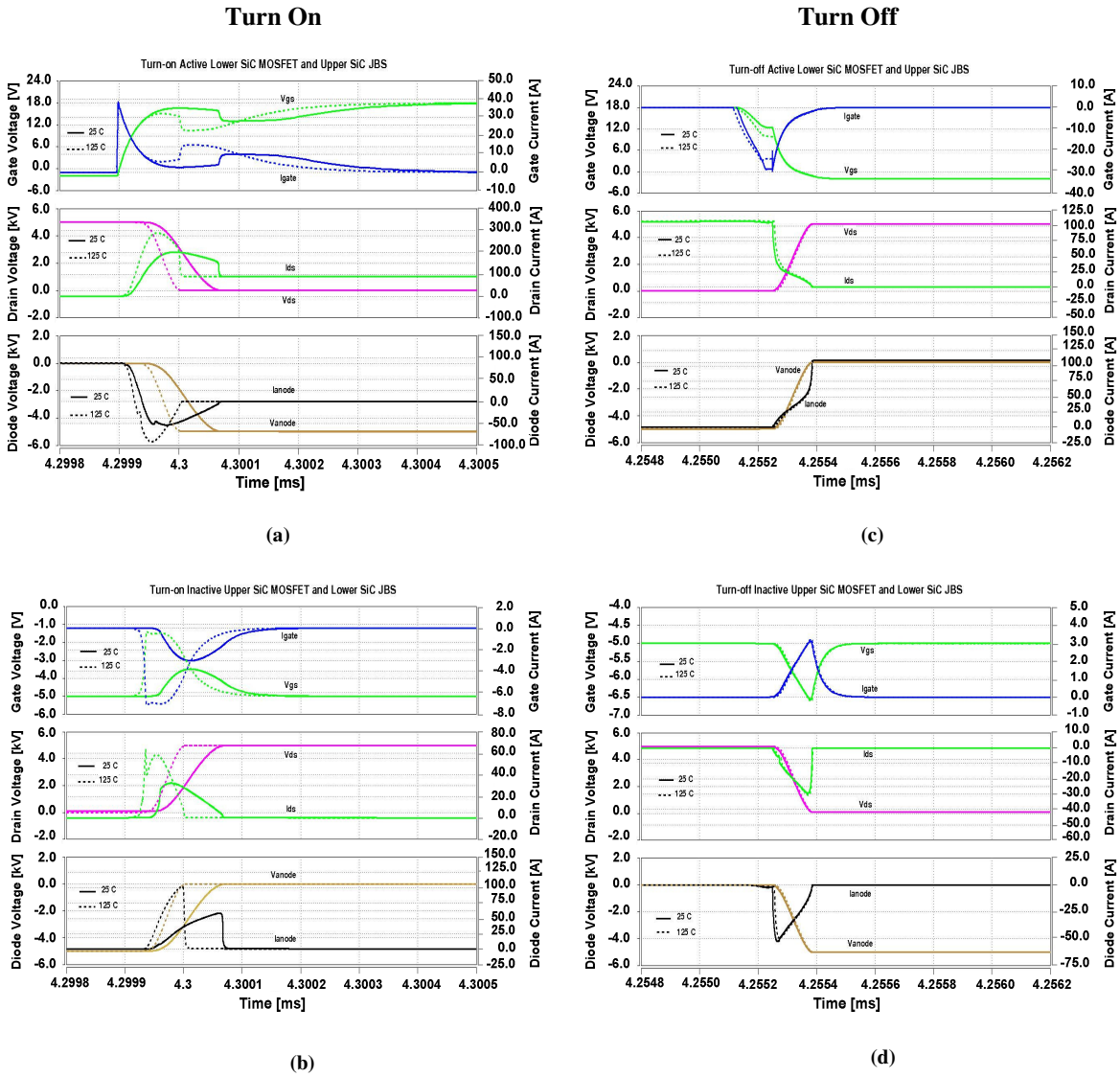

Fig. 7: Simulated results at 25 °C (solid) and 125 °C (dashed): (a) Turn-on waveforms for the active lower MOSFET gate voltage and current, drain voltage and current, and active upper diode current and voltage; (b) Turn-on waveforms for the inactive upper MOSFET gate voltage and current, drain voltage and current , and inactive lower diode current and voltage; (c) Turn-off waveforms for the active lower MOSFET gate voltage and current, drain voltage and current, and active upper diode current and voltage; (d) Turn-off waveforms for the inactive upper MOSFET gate voltage and current, drain voltage and current, and inactive lower diode current and voltage.