High-Voltage, High-Frequency SiC Power MOSFETs Model Validation*

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Abstract- **Circuit simulator model validation procedures and results are presented for SiC power MOSFETs. The characteristics discussed include on-state conduction, resistive load switching, inductive load switching, and high voltage depletion capacitance. The validation procedures are performed using a script written in the AIM language that is incorporated in the Saber®♦ circuit simulator. The script uses the model parameter sets from the IGBT Model Parameter ExtrACTion (IMPACT) tools to perform simulations and then compares the simulated results with measured characteristics. Example validation results are presented for recently developed 5 A, 10 kV SiC power MOSFETs demonstrating for the first time the model performance at the full application switching voltage (5 kV for the 10 kV devices).**

I. INTRODUCTION

Recent advances in the silicon carbide (SiC) materials and fabrication processes have led to the development of high-voltage, high-frequency (HV-HF) power devices that have 10 kV, 20 kHz switching capability [1, 2, 3]. The emergence and continuous improvement of SiC HV-HF devices is expected to revolutionize commercial and military electric power transmission and distribution systems by extending the use of switch-mode power conversion to high-voltage applications. Furthermore, the market of SiC power devices promises to grow considerably in the future due to the implementation of SiC-based power converters, such as motor drives for automotive applications, inverters for wind and solar power systems, and power factor correction (PFC) circuits for switch-mode power supplies.

Computer simulation is an important step during the design and implementation of power electronic converters using SiC power devices. In order to perform such simulations, accurate models emulating the transient and steady-state behavior of SiC power devices are needed. The Hefner MOSFET model in [4] was extended in [5] to include specific temperature-dependent material properties of SiC. It was then used to describe the performance of a 2 kV, 5 A 4H-SiC power MOSFET. Furthermore, reference [6] extended the IMPACT model parameter extraction tools described in [7] to include SiC material properties and also included the high voltage capacitance measurement procedures needed for high voltage SiC power devices.

In this paper, the SiC MOSFET Saber™ model and the model parameter extraction sequence are applied to 10 kV SiC power MOSFETs for the first time, and the simulation results are validated using measurements from well characterized experimental test systems [8]. The new model validation procedure is implemented using automated macro procedures to facilitate comprehensive validation of SiC power MOSFET devices. Using these automated procedures, validation results are routinely obtained for the various power MOSFETs produced by the DARPA Wide Bandgap Semiconductor Technology - High Power Electronics (WBST-HPE) program.

II. POWER MOSFET MODEL VALIDATION PROCEDURE

The automated model validation procedures are implemented using a macro script written in the AIM language incorporated in the Saber™ circuit simulator. The script automatically loads and displays the complete set of data from each laboratory measurement procedure and then performs the simulation for comparison with the measurements. The simulations are performed using the MOSFET parameters that are automatically loaded from the IMPACT extraction files.

The following subsections describe the validation results obtained for a sample 10 kV SiC power MOSFET developed under the DARPA HPE Phase-2 program. The characteristics discussed include on-state conduction, resistive load switching, inductive load switching, and gate charge characteristics. The inductive and resistive switching measurements are performed in the laboratory using a specially designed high voltage switching test system [8].

A. On-State Characteristics

Fig. 1 shows measured (dashed) and simulated (solid) output characteristics for the 10 kV SiC MOSFETs. These results are for temperatures of (a) 25 ºC, (b) 125 ºC, and (c) 200 ºC. The curves are linear in the on-state region and have a pronounced change in curvature as the saturation or pinch-off region is approached. This occurs because the device has a large epitaxial layer resistance in series with the MOSFET channel, and the channel has a high transconductance.

♦ Saber® mixed-technology system simulation software is a registered trademark of Synopsys®, Inc. Certain commercial products or materials have been identified in order to specify or describe the subject matter of this paper adequately. This does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products are the best for the purpose.

At 125 ºC and 200 ºC, there is less of a reduction in on-state resistance with temperature than for Si. This occurs because the effective channel mobility does not decrease with temperature for SiC as it does in Si. In the SiC MOSFETs, the channel mobility actually increases with temperature as more interface traps become occupied with the larger concentration of electrons available for conduction. The bulk mobility decreases with temperature in both SiC and Si as the temperature increases from 25 ºC to 200 ºC due to increased carrier scattering [4]. The resulting effect for SiC is a decrease in channel resistance that compensates for the increase in the drift layer series resistance.

B. Inductive Load Switching

Fig. 2 shows the measured (dashed) and simulated (solid) clamped inductive load turn-off waveforms for three different inductor current levels (4 A, 6 A, and 8 A). The waveforms are for a clamp voltage of V_c = 5 kV. Their respective turn-off times are 50 ns for the 8 A case, 70 ns for the 6 A case, and 100 ns for the 4 A case.

The simulated test circuit of Fig. 3 emulates the well-characterized test circuit using: a gate resistor of 4 ? , a gate driver voltage pulse (V_g) having a 12 ns fall time from 20 V to 0 V, a variable dc inductor supply voltage (V_{dd}) used to adjust the drain current level, a drain inductor of 1.92 mH, an inductor series resistance of 10 ? , a diode plus load inductor capacitance of 20 pF, a gate-drain package capacitance of 5 pF, and a drain-source package capacitance of 20 pF.

C. Resistive Load Switching

Fig. 4 shows the measured (dashed) and simulated (solid) turn-on waveforms of a SiC MOSFET under resistive load conditions for different values of gate resistance. Fig. 5 shows the turn-off waveforms for the same device and circuit conditions. The simulated test circuit of Fig. 6 emulates the well-characterized measurement circuit using: a gate driver voltage pulse (V_g) with a 12 ns rise time and a 12 ns fall time from 0 V to 20 V, a drain series resistor value of 1.2 kΩ, a drain supply voltage of V_{dd}= 5 kV, a gate-drain package capacitance of 5 pF, and a drain-source package capacitance of 20 pF. The power MOSFET gate drive resistor was varied to provide different switching speeds.

It is well known that the gate resistor affects the turn-on delay and current rise time as well as the turn-off delay and voltage rise time. This is reflected in the results shown in Fig. 4, where the turn-off delay is about 65 ns, 105 ns, 195 ns, and 380 ns, and the turn-off current fall time (90 % to 10 %) is about 130 ns, 140 ns, 200 ns, and 350 ns for the gate resistance values of 7 Ω, 13 Ω, 26 Ω, and 53 Ω, respectively.

D. Gate-Charge Capacitances

Fig. 7 (a) shows an example of the measured gate voltage and gate current waveforms used to generate the gate charge characteristics. Fig. 7 (b) shows the simulated (solid) and measured (dashed) gate-charge characteristics for three different values of drain-to-source supply voltages which are 10 V, 100 V, and 400 V, respectively. The gate charge characteristics are obtained for a relatively constant gate current pulse and a high-valued drain resistance of approximately 10 kO. The relatively constant gate current is generated using a 100 V pulse with a large gate resistor (5 kO for a 5 A device).

One notable difference between the gate charge characteristics of SiC compared to Si is that SiC has a wider gap between the extrapolated low- and high-gate voltage regions (difference indicated in Fig. 7 (b)) due to the larger built-in potential (V_{bigd}) of the gate-drain overlap region: V_{bigd}= 2.8 V for SiC, while V_{bigd}= 0.8 V for Si with a high doped gate drain overlap region.

III. CONCLUSIONS

In this paper, a validation procedure for the output characteristics, resistive and inductive load switching, and gate charge behavior are presented for power MOSFETs and demonstrated for 10 kV SiC devices. The validation procedures are performed using a macro script written in AIM language incorporated in the Saber™ circuit simulator, thus automating the process of running the simulations and loading results for comparison with measurements. The similarity of measured and simulated results demonstrates the accuracy of the IMPACT parameter extraction software tools, the SiC MOSFET model implemented in the Saber™ circuit simulator, and the test system circuit parameter values.

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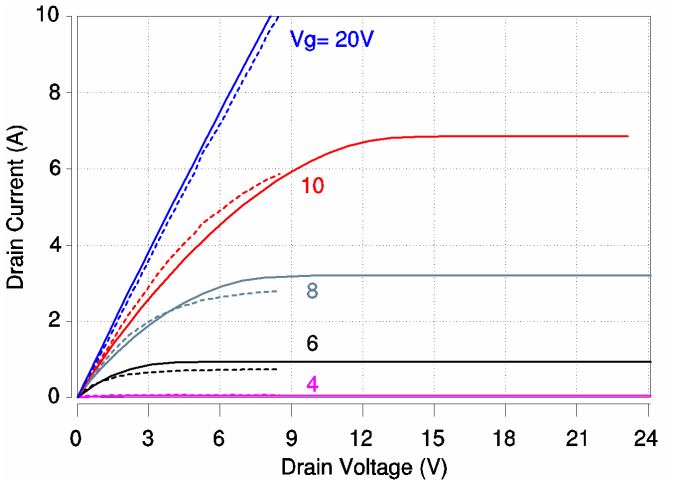
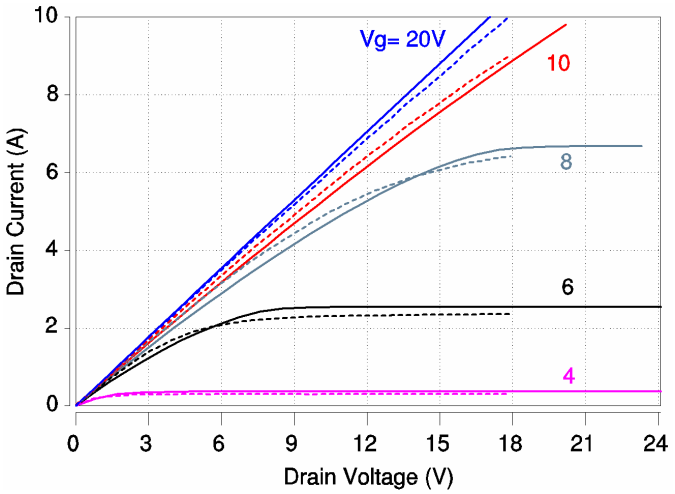


(a)



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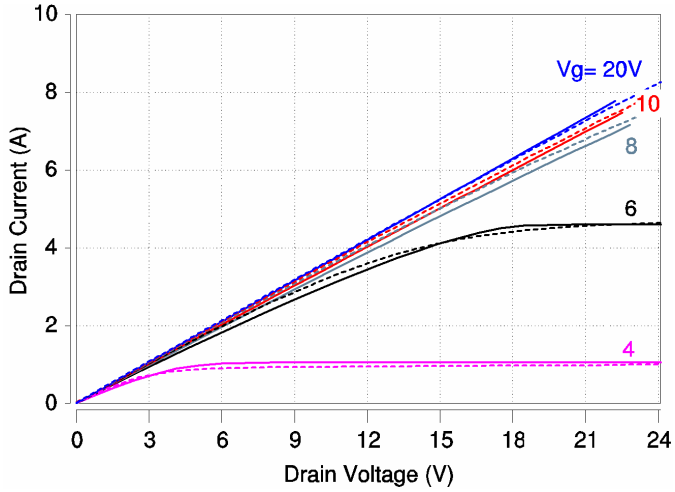
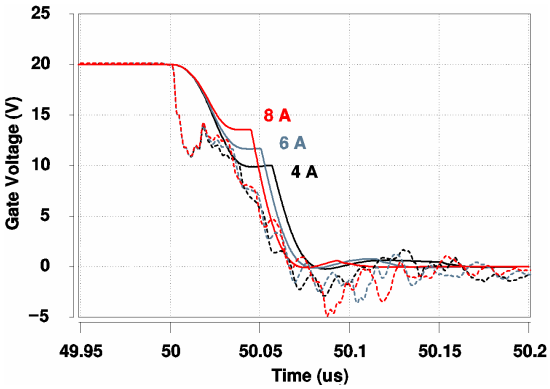
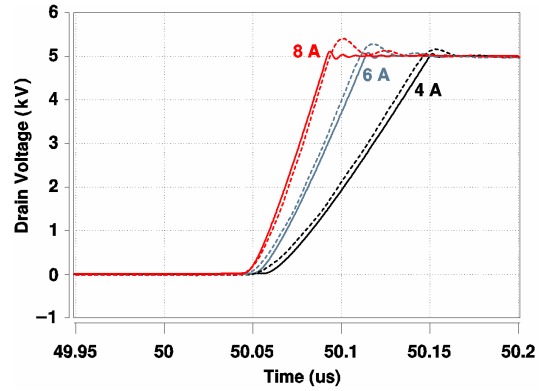


(c)

Figure 1. Comparison of measured (dashed) and simulated (solid) output characteristics at 25 ºC (a), 125 ºC (b), and 200 ºC (c) for a 5 A, 10 kV SiC MOSFET.



(a)



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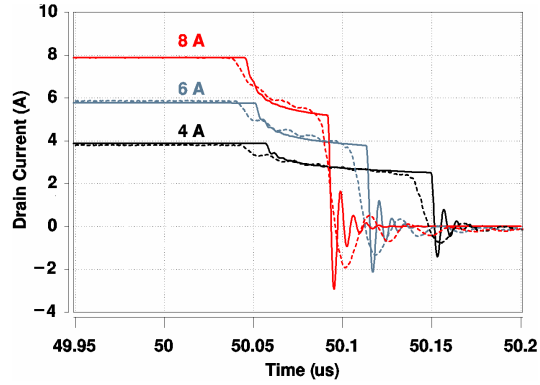


(c)

Figure 2. Comparison of measured (dashed) and simulated (solid) inductive-load switching turn-off waveforms at 25 ºC for a clamp voltage of 5 kV and a 5 A, 10 kV SiC MOSFET: (a) gate voltage, (b) drain voltage, (c) drain current.

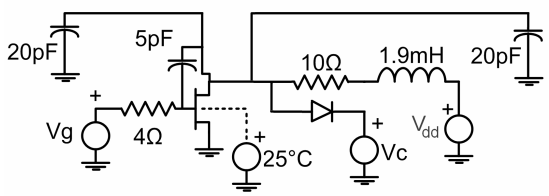
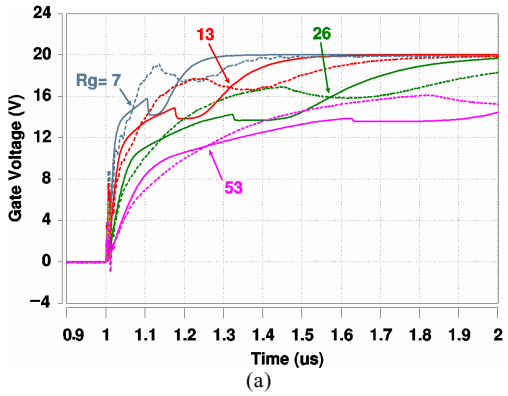
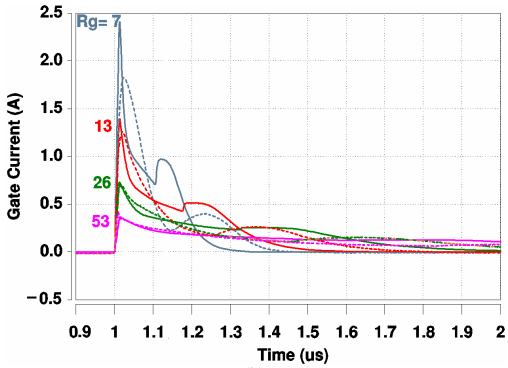


Figure 3. Circuit used for inductive load simulation where the V_g pulse width is 50 µs, V_c is 5 kV, and V_{dd} is 175 V, 260 V, and 355 V to obtain the drain currents of 4 A, 6 A, and 8 A, respectively.



(a)



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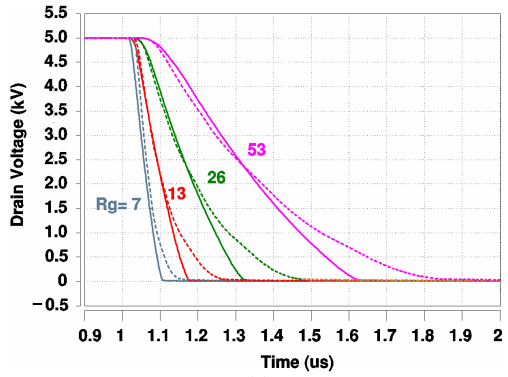

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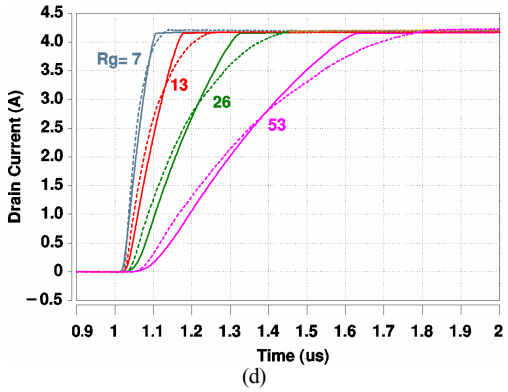
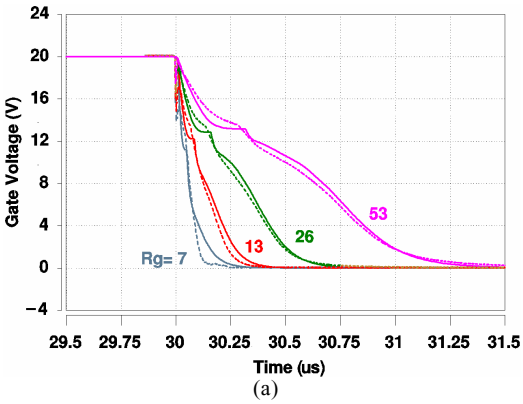
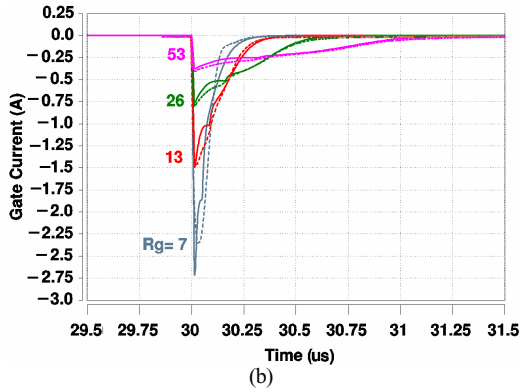


(d)

Figure 4. Comparison of measured (dashed) and simulated (solid) resistive-load switching turn-on waveforms at 25 ºC for a 5 A, 10 kV SiC MOSFET : (a) gate voltage, (b) gate current, (c) drain voltage, and (d) drain current.



(a)



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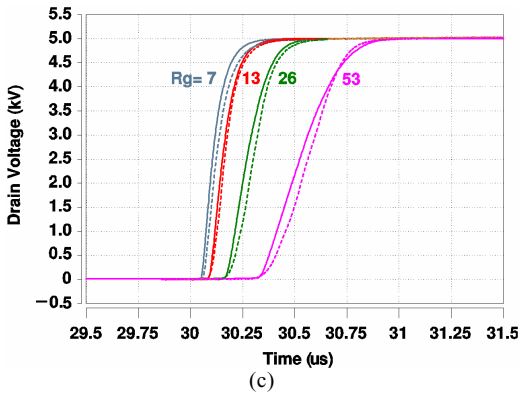

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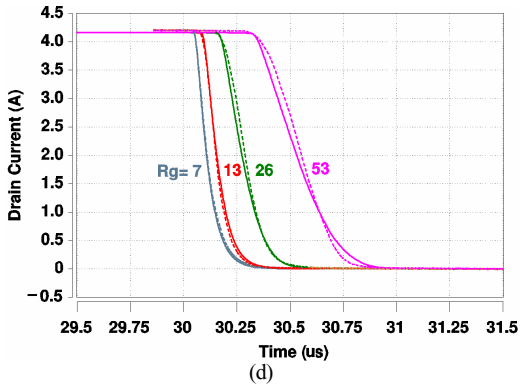


(d)

Figure 5. Comparison of measured (dashed) and simulated (solid) resistive-load switching turn-off waveforms at 25 ºC for a 5 A, 10 kV SiC MOSFET : (a) gate voltage, (b) gate current, (c) drain voltage, and (d) drain current.

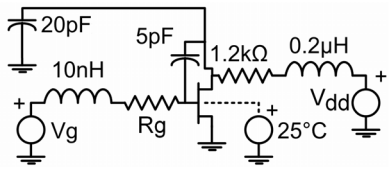
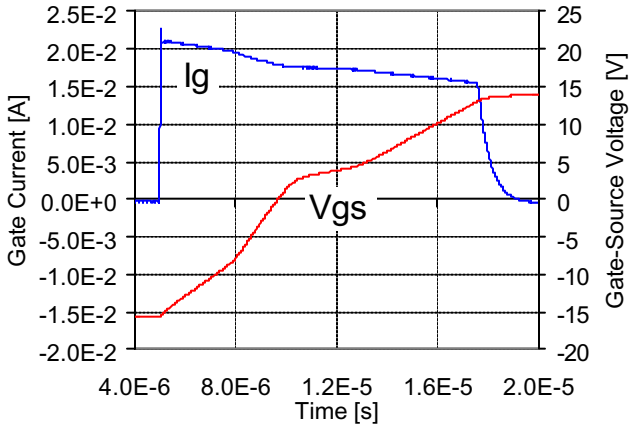
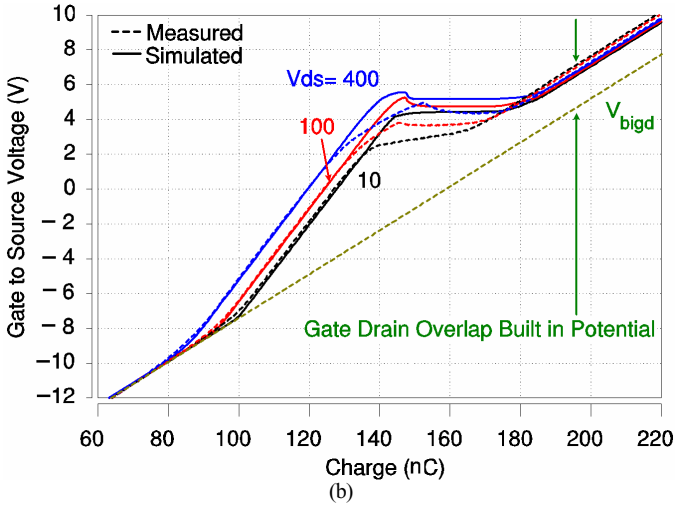


Figure 6. Circuit used for resistive-load switching simulation circuit where V_{dd} is 5 kV, V_g is pulsed from 0 to 20 V with a 12 ns rise and fall time, and R_g is varied to obtain the different switching speeds.



(a)



(b)

Figure 7. a) Waveforms used to generate the gate charge characteristics, and b) comparison of measured (dashed) and simulated (solid) gate charge plots at 25 ºC for a 5 A, 10 kV SiC MOSFET.