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Silicon nanowire on oxide/nitride/oxide for memory application

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Abstract
We report the fabrication and characterization of Si nanowire memory devices with oxide/nitride/oxide stacked layers as the gate dielectrics and charge storage media. The devices were fabricated by using photolithography to pattern the metal contacts to the Si nanowires grown on pre-defined locations. A large memory window with high on/off-state current ratio due to the small radius and intrinsic doping of the Si nanowire is obtained. In addition, the simple reversible write/read/erase operations have been implemented with these memory devices. The dynamics of the nanowire/nitride charge exchange and its effect on the threshold voltage and memory retention have been investigated.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Nanowires and nanotubes have been of great interest for their potential applications in the next generation nanoelectronics as they represent the ultimate medium which allows efficient charge transport. Such intrinsic nanoscale materials have been intensively investigated to extend the scaling of the metal oxide semiconductor field effect transistor (MOS FET) beyond its generic integrating density and functionalities [1]. Different strategies to develop nanowire test structures have been demonstrated, including nanoelectromechanical systems, photoelectric devices and bio-sensors [2–4]. Among the various approaches, the application of nanowires for non-volatile memory, such as FLASH and semiconductor–oxide–nitride–oxide–semiconductor (SONOS) devices, is especially interesting because of the intrinsic scalability of the nanowires. There have been recent reports of nanowire-FET-based non-volatile memory with self-assembled molecules or ferroelectric thin film as the charge storage media [5–8]. These advanced approaches showed very interesting device properties; however, the molecule is relatively unstable at high temperature, and the integration and scaling-down of ferroelectric film with CMOS materials/processes are considerably difficult [1]. In this study, we fabricated and characterized nanowire memory devices consisting of a silicon nanowire (SiNW) on stacked oxide/nitride/oxide (ONO) layers, which act as the back gate dielectrics and charge (i.e. information) storage media. (These devices are named SiNW ONO devices hereafter.) Stacked ONO dielectrics are regularly used for non-volatile memory devices for much higher reliability compared to FLASH device [9]. This approach is engaged to provide a smooth transition for integrating SiNW into viable memory devices within the well known SONOS structure. In addition, the SiNW ONO device exhibits reliable write/read/erase operations with a large memory window and high on/off current ratio, $\sim 10^5$, which are highly advantageous for applications in non-volatile memory.

2. Experimental details

We fabricated the SiNW ONO memory devices with the Si nanowires grown from the Au catalyst on the pre-defined locations on the ONO surface. First, a thermal SiO_2 of 30 nm

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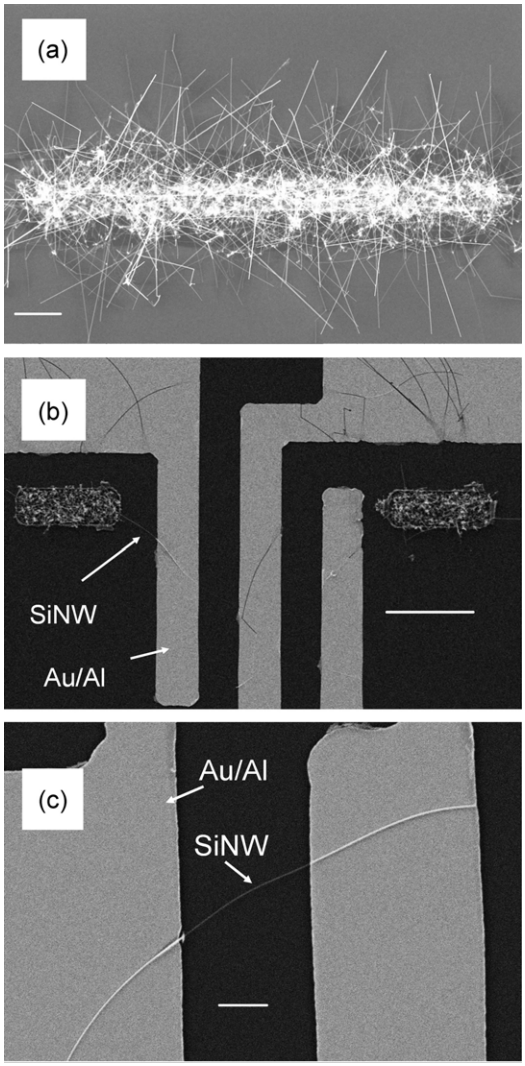

Figure 1. (a) Scanning electron microscopic image of the SiNW grown from the rectangular-patterned Au catalyst (scale bar: 10 μm); (b) metal contacts patterned on *in situ*-grown SiNWs (scale bar: 10 μm); (c) a typical SiNW ONO device (scale bar: 1 μm).

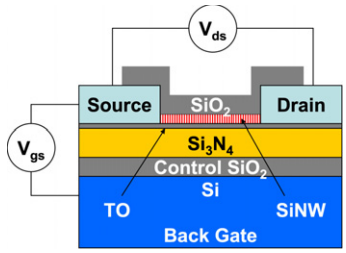

Figure 2. A schematic drawing of the SiNW ONO device structure cross-section and electrical measurement set-up.

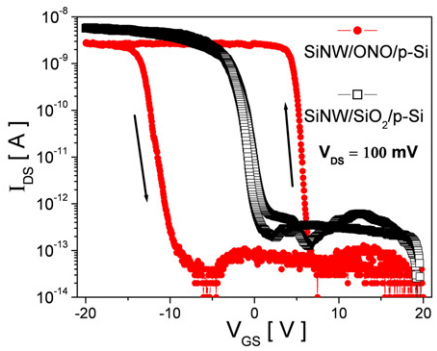

Figure 3. Typical drain current versus gate voltage characteristics of the SiNW ONO device and regular SiNW FET control device. A large hysteresis (i.e. memory window) was observed for the SiNW ONO device while there was no significant hysteresis observed for the control device.

was thermally grown on the p-type silicon (p-Si) substrate as the tunnelling-blocking control oxide (CO) followed by 60 nm low-stress silicon nitride prepared by a low-pressure chemical vapour deposition (CVD) at 650 °C. A thin oxide (∼2 nm) was deposited on the Si_3N_4 by plasma enhanced CVD as the tunnelling oxide (TO). Then an Au film (∼1 nm) was defined on the ONO surface as the catalyst by using the photolithography and metal lift-off processes. The SiNWs were grown in a CVD furnace, at 420 °C, under 500 mTorr SiH_4 via a vapour–liquid–solid mechanism [10–12]. SiNWs of 5–50 nm in diameter and 10–60 μm in length were obtained. Figure 1(a) shows the scanning electron microscopy (SEM) image of the SiNWs grown from the rectangular-patterned Au catalyst.

We then used the following compatible processes to pattern the metal contacts (i.e. source and drain of the nanowire FET) on the catalyst-grown nanowires as shown in the SEM image of figure 1(b). We first spin the lift-off resist (LOR) and photoresist (PR) on the substrate (with nanowires) and define the contact patterns with photo-alignment, exposure and resist developing. The stacked Au/Al layers were then deposited by thermal evaporation and defined by a metal lift-off process. Statistically, more than 40% of the metal patterns contact to one or more nanowires. Finally, the devices were encapsulated with sputtering Si oxide (∼30 nm) at room temperature to protect the nanowires from the external environment (air and water). A typical SEM image of an SiNW ONO device is shown in figure 1(c). In addition, regular back-gate SiNW FETs with only SiO_2 (∼30 nm in thickness) as the gate dielectric have also been prepared as control devices for comparison.

3. Results and discussion

A schematic drawing of the SiNW ONO device structure cross-section and measurement set-up is shown in figure 2. The typical electrical characterization, source–drain (I_{DS}) current versus gate voltage (V_{GS}) of a SiNW ONO device and a regular SiNW FET control device at 100 mV source–drain voltage (V_{DS}), is shown in figure 3. The SiNWs are about 20 nm in diameter and 3 μm in channel length. A large hysteresis (i.e. memory window) was observed from the SiNW ONO device while there was no significant hysteresis observed from the control device. It can be explained as follows: at a high positive back gate voltage (e.g. 20 V), the negative charges (i.e. electrons) are tunnelling from the nanowire, through the thin TO, to the dielectrics and stored in the oxide/nitride interface and nitride [9]. These negative charges acting as a

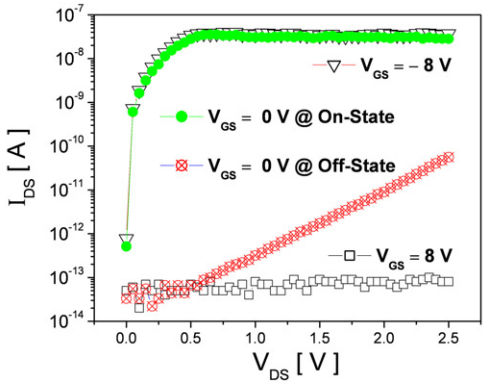

Figure 4. Typical I_{DS}–V_{DS} curves of the SiNW ONO device at $V_{GS} = \pm 8$ V and at $V_{GS} = 0$ V in the on and off states with high current on/off ratio.

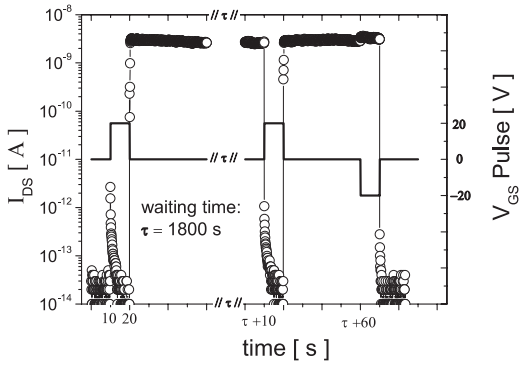

Figure 5. Simple reversible *write*, *read* and *erase* operations of SiNW ONO devices are implemented by using programming voltage pulses of $V_{GS} = 20$, 0 and -20 V, respectively. The I_{DS} is kept measuring (i.e. reading) at $V_{DS} = 100$ mV.

compensating negative gate voltage induce a positive threshold voltage (V_t) shift, and hence the SiNW ONO device is turned on at a higher positive gate voltage than the regular SiNW FET. As the gate voltage switches to negative, the negative charges tunnel out of the ONO stacked layers and positive charges start to store in the ONO stacked layers at a higher negative gate voltage (e.g. -20 V). The positive charges acting as an effective compensating positive gate voltage induce a negative V_t shift, and hence the device is turned off at a more negative gate voltage than the regular SiNW FET.

The injected charges were stored in the ONO stack under and beside the SiNW, inducing a large V_t shift. The effective injected charge density can be calculated as $\sim 10^{11}$ cm^{-2} for a V_t shift of 6 V. The relatively low on-state current ($\sim$3 nA) is due to the un-doped long SiNW channel ($\sim 3\ \mu$m) and high contact resistance between the un-doped SiNW and source/drain metal, which we have previously reported [13].

Figure 4 shows the I_{DS}–V_{DS} curves at $V_{GS} = \pm 8$ V and at $V_{GS} = 0$ V in the on and off states. The SiNW ONO device is turned on and off like the regular SiNW FET by the gate voltages of $V_{GS} = -8$ V and $V_{GS} = 8$ V, respectively, with a current on/off ratio $\sim 10^6$ at $V_{DS} = 0.5$ V. Then the I_{DS}–V_{DS} curves are measured at $V_{GS} = 0$ V for the on and off states obtained by using write and erase voltage pulses of $V_{GS} = +20$ and -20 V, respectively, with 1 s programming time. The current ratio between the on and off states is about 5×10^5 at $V_{DS} = 0.5$ V. Note that off-state current increases with V_{DS} as more stored charges tunnel out of the charge trapping layer at higher V_{DS} [14, 15].

As shown in figure 5, simple reversible *write*, *read* and *erase* operations of the SiNW ONO device are implemented by using programming voltage pulses of $V_{GS} = 20$, 0 and -20 V, respectively. During the operation, the I_{DS} is kept sampling (i.e. reading) at $V_{DS} = 100$ mV. The device is first measured at $V_{GS} = 0$ V with very low off-state I_{DS} current since no charges are stored in the nitride. From the 10th second, a 10 s pulse of 20 V is applied on the gate to drive negative charges to tunnel from the SiNW and store in the ONO layers. Low I_{DS} was observed during this write operation at $V_{GS} = 20$ V. These stored negative charges shift the V_t to positive 7.5 V according to the I_{DS}–V_{GS} curve in figure 3. From the 20th to the 60th second, the device is read at $V_{GS} = 0$ V with high on-state I_{DS}. During the continuous 1000 time reading operation for a total of 40 s, the on-state current decays $\sim$8%, resulting from the loss of a certain number of charges from the nitride layer. The loss of charge is due to the thin TO between the SiNW and the nitride, and the read-disturb mechanism [14]. The device was then placed in an open circuit and re-measured after a waiting time ($\tau = 1800$ s). The current is almost equal to the value measured before waiting, indicating good memory retention, and the memory retention was disturbed by the reading operation. The *write* and *read* operations have been repeated from $\tau + 10$ to $\tau + 60$ s and the same behaviours have been observed. From $\tau + 60$ s, a 10 s pulse of -20 V is applied on the gate to drive the positive charges (i.e. holes) to tunnel from the SiNW and store in the ONO layers. High I_{DS} is obtained during the *erase* operation due to the high negative gate voltage; however, the V_t is shifted to -5.0 V by the stored holes according to the I_{DS}–V_{GS} curve in figure 3. From $\tau + 70$ s (after the *erase* pulse), low off-state current is read at $V_{GS} = 0$. Note that permanent degradation in current and V_t shift is observed after 10^5 write/erase cycles due to the low quality of deposited tunnelling oxide, which can be improved in future study.

4. Conclusion

We have fabricated SiNW ONO non-volatile memory devices based on CVD-grown nanowires and a self-alignment technique. The devices demonstrate large memory window, high on/off ratio and reversible *write*, *read* and *erase* operations with considerable retention and endurance, which are highly advantageous for applications in non-volatile memory. In addition, the SiNW ONO device structure provides a well defined platform to investigate the intrinsic properties of the nanowire.

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