A CUSTOM INTEGRATED CIRCUIT COMPARATOR FOR HIGH-PERFORMANCE SAMPLING APPLICATIONS

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Abstract - This paper reports on the design and performance of an application specific integrated circuit (ASIC) comparator that has been optimized for equivalent-time waveform sampling applications. The comparator, which has been fabricated with an 8.5 GHz f_T, bipolar silicon process, features a bandwidth of >2 GHz, a settling-time accuracy of 0.1% in 2 ns, and almost total elimination of "thermal tails" in the settling response. Several novel design features that have been used to achieve this level of performance are presented. The comparator can be used in a sampling system for both frequency domain measurements, e.g. wideband rms voltage measurements, and high accuracy time domain pulse measurements.

INTRODUCTION

Research at NIST (National Institute of Standards and Technology) and several other laboratories has demonstrated that very high performance equivalent-time sampling of repetitive waveforms can be achieved with a high-speed, latching analog comparator used as a sampling device in a technique generally referred to as Sampling Comparator System (SCS) [1,2,3]. Similar to digital sampling oscilloscopes, SCS's are equivalent-time sampling systems that are generally configured in either one of two elegantly simple circuits as illustrated in fig. 1. [1,2,3].

Since the successive approximation method shown in fig. 1(b) was used as a test bed for the work described in this paper, it will be instructive to review briefly the operation of that approach. This method implements an A/D conversion in equivalent-time by means of a comparator that provides the sampling function as well as the decision function. As illustrated, the strobed comparator is operated in a feedback loop to sample repetitively the input signal at a given instant on the waveform. The comparator compares the reference voltage applied to one input with the instantaneous value of the input waveform at the time the comparator is strobed. Based on the output state of the comparator, the successive approximation register (SAR) instructs the digital-to-analog converter (DAC) to increment or decrement the level applied to the reference input of the comparator in preparation for the next comparison. The process is repeated until the reference level equals the sampled level of the waveform to the desired degree of precision. Then, the strobe position is moved to another point on the waveform and the search routine is repeated. This sampling process is continued until a desired record of samples has been obtained. Any arbitrary, repetitive waveform can be measured with the SCS; however, one of the main virtues of the SCS is its exceptional accuracy in the measurement of step-like waveforms. In particular, we are interested in the ability of the SCS to accurately track and settle on the fast transition edge of such waveforms

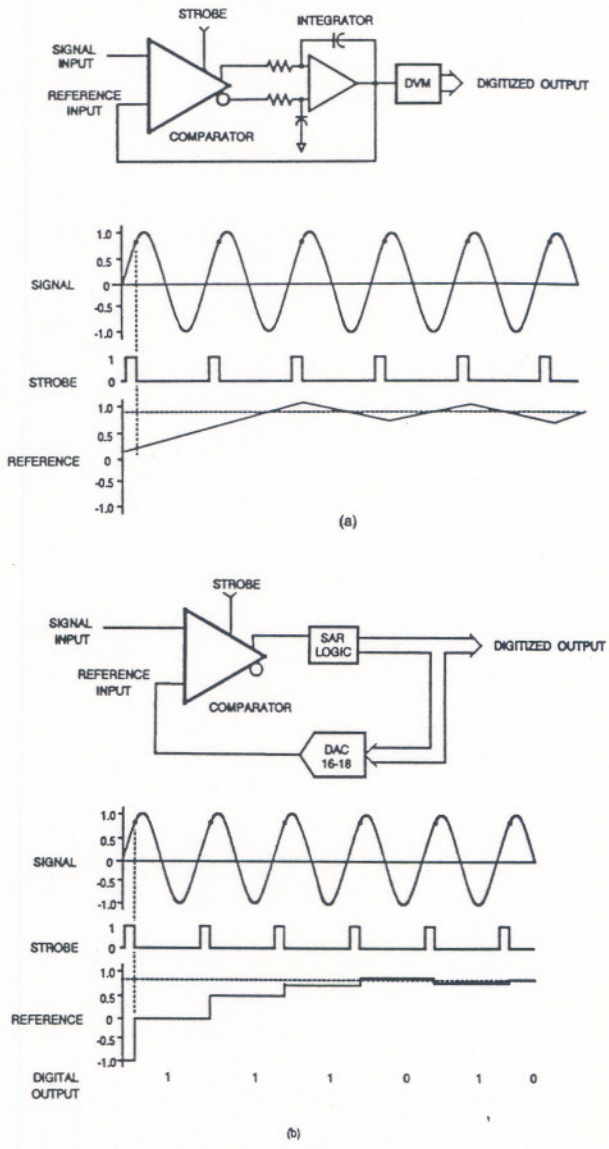

Fig. 1. Two commonly used sampling comparator circuits, with diagrams illustrating the search routines used for controlling the reference input voltage: (a) the sampling voltage tracker, and (b) the equivalent-time successive approximation A/D converter.

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At least one manufacturer markets a general purpose waveform analyzer based on the SCS approach just described. This instrument is configured such that the comparator is housed separately in a small probe connected by an umbilical cable to a mainframe containing the rest of the system. This arrangement permits the sampler to be connected directly to the output of the source of voltage to be measured, eliminating the need for connection cables and the encumbrance of the supporting hardware. The instrument provides a reference voltage to a resolution of 16 bits with an equivalent time resolution of 10 ps, in addition to other features that make waveform measurement and processing very easy. We have used this commercial instrument with our own probe circuit as a means of evaluating and reporting the performance of our custom ASIC comparator.

COMPARATOR DESIGN CONSIDERATIONS

The impressive performance of SCS's in current use has been achieved with inexpensive, commercially available IC comparators, but the performance of the system is almost entirely determined by the comparator. Because the comparators that are generally available for this purpose have not been optimized for this application, there is a potential for significant improvement in performance by developing a comparator specifically designed for SCS's. Initially, GaAs technology was investigated for a custom comparator because of the inherent high-speed characteristics and high input impedance. However, the high-speed characteristic is offset by a number of persistent problems such as backgating and channel conductance dispersion which limit the usefulness in precision analog applications [4]. Silicon devices, although not as fast as GaAs devices, can still provide competitive speeds. A high-performance silicon wafer process with bipolar devices having a typical f_T = 8.5 GHz was selected for our ASIC comparator. The manufacturer offers these high speed bipolar transistors configured in uncommitted arrays together with resistors, capacitors, JFET's, and Schottky diodes. The devices are contained on a 1.45 mm by 1.45 mm substrate allowing for the economical integration of small, very high performance circuits. Before the design was committed to fabrication, extensive simulations of the design were performed with models provided by the integrated circuit foundry.

The conflicting requirement for a comparator of both high gain and wide bandwidth can be realized by relying on the regenerative amplification of a latch stage while minimizing the amount of preamplification. Fig. 2 shows a simplified diagram of the custom comparator to illustrate this concept. The first stage is a low-gain differential amplifier that compares the input signal with the reference level and amplifies the difference. The second stage is a master latch that samples the amplified signal from the first stage. When the latch stage is activated (i.e. the current source is switched from track to latch), the positive feedback will amplify any small difference from the first stage. The regenerative growth of the initial difference voltage will finally be limited by the current available to the latch so that one device becomes fully on and the other completely off, resulting in a latching of the stage. Thus, the latch stage serves two important functions: regenerative amplification and latching or holding the state of comparison at the sampling moment. Minimizing the gain of the first stage not only improves the bandwidth but lessens the overload recovery time and attendant signal amplitude dependent

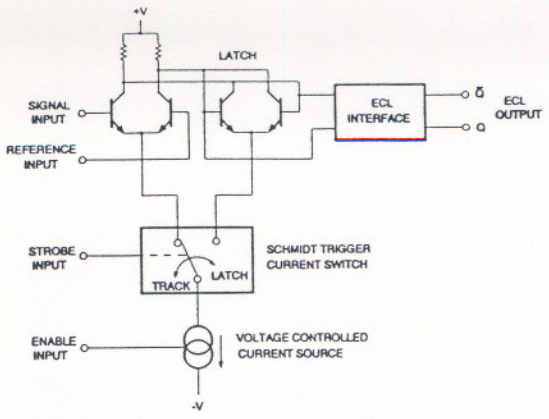

Fig. 2. Simplified block diagram of the custom integrated circuit comparator.

delay. Any dispersion in the delay of the first stage will cause harmonic distortion. Actually, in this application the first stage can be considered more as a high-speed differential gate rather than an amplifier. The trade-off for this approach is replacement of the equivalent comparator gain by a finite delay time during which small difference signals must regenerate exponentially to higher voltage levels in the latch stage. An approximation of the time-gain relationship [5,6] is given by

$$t = \tau \log(A). \qquad (1)$$

where A is the equivalent gain of the latch stage defined as the ratio of the latched differential output voltage to the differential input voltage at the sampling moment, and τ is the regeneration time constant of the stage. The value of τ was determined from simulation to be about 130 ps. For example, a latched differential output voltage of 0.4 volts and a 100 μV differential input voltage at the sampling moment (a gain of 4000) will require over 650 ps for the latch output voltage to reach 0.4 volts. However, the total regeneration time is not an issue in equivalent-time sampling because of the relatively long time between samples. In the early regenerative phase of the latch stage, however, the amount of hystersis is small so that the stage is sensitive to disturbances such as noise or amplifier "blow by" which may have sufficient energy actually to reverse the polarity of initial exponential growth causing both random and systematic errors. "Blow by" is referred to here as the effect of the signal coupling through the first stage after it has been deactivated. From the standpoint of reducing errors, it is desirable to design the latch stage for the minimum regeneration time constant, τ so that the stage latches as fast as possible.

The speed at which the transition is made from track to latch is important for high slew rate signals. This transition time defines the effective sampling aperture which not only determines the equivalent bandwidth of the comparator, but also influences the harmonic distortion produced from a sampled waveform [7]. To take advantage of the inherent fast regeneration time constant of the latch stage and make it less dependent on the strobe source transition-time, a Schmidt trigger current switch was designed on the chip as part of the comparator. Simulation studies of the Schmidt trigger current switch indicate about a 75 ps (10-90%) transition-time for the current to switch to the emitters of the latch stage.

A common observation with commercial comparators is that when step-like waveforms are being sampled, longer term (>100 ns) settling time errors are observed. Often these errors amount to several millivolts and may require up to one microsecond to settle out. This phenomenon is often referred to as a "thermal tail" error, which is a nonlinear process that manifests itself in the time domain but also can cause significant signal level dependent errors in the frequency domain. The "thermal tail" problem is exacerbated in fast comparators because of the higher operating currents that are required. The problem arises because the transistors of the input differential pair conduct unequally, except when the input and reference signals are equal. Since the input signals to the comparator are dynamic and usually unequal except at the sampling instant, the difference can be large enough to turn one transistor fully on while the other is turned completely off. This state will unbalance the power dissipation and attendant heating of each transistor from the equal input condition. Because of imperfect thermal coupling between the two transistors, the transistor base-emitter junctions will be at different temperatures. Consequently, the base-to-emitter potentials of the differential pair will differ and will not track with time until many thermal time constants have elapsed. This leads to an offset error as a function of time between the reference voltage and the input voltage which manifests itself as a settling time error. Convincing evidence of this effect can be observed from the variability of the settling time that occurs when the duty-factor of the signal is changed.

Enabling Technique

A new hardware design approach for eliminating the thermal errors and other errors due to long response time anomalies has been incorporated in the custom comparator. The approach is based on an enabling technique that activates the differential devices within the comparator for only a short interval before being strobed. Refer again to fig. 2 which shows a voltage controlled current source that can be turned on by an enable input signal. The idea here is to keep the emitter current to the differential pair off most of the time and to energize the stage just before a comparison is required. Keeping the input stage off most of the time, and then enabling for a short period, minimizes the power dissipated in the transistors and the resulting temperature differences. In this way the differential amplifier is 'on' for a period only long enough to track the difference between the signal and the reference voltage. After the current source has been turned on for a period, the strobe signal switches the current source from the first stage to the latch stage. The lead-time between the enable and strobe is set at about 2 ns, which was shown by simulation and practice to be sufficient for the stage to accurately track a difference before strobing. In our application the comparator is strobed at about a 30 kHz rate, which amounts to a very low thermal dissipation duty-factor for the first stage.

The effectiveness of the enabling technique in improving the settling time response of our custom comparator used in the SCS system is shown in fig. 3. In fig. 3(a) the enabling was deactivated so that the voltage controlled current source of fig. 2 remains continuously on. Note that over 200 ns are required to settle to the final DC value. Fig. 3(b) shows the rather dramatic improvement in settling time when the enabling technique is activated. The enabling system can have a similar profound influence in improving the

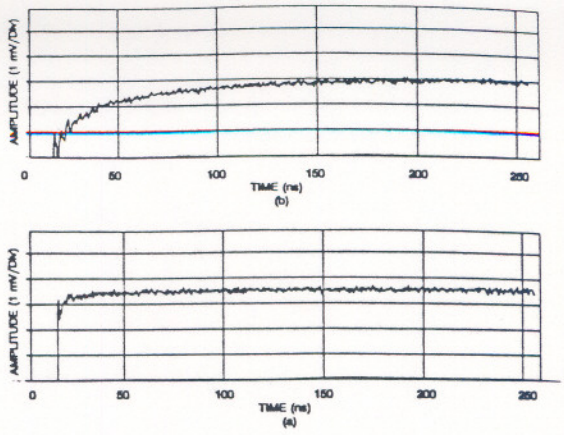

Fig. 3.(a) Settling-time response of the sampling comparator system with the enabling system of the comparator deactivated so that the current source of fig. 2 remains continuously on. (b) The much improved settling-time response by enabling the comparator 2 ns before strobing.

flatness of the overall frequency response, at frequencies corresponding to the thermal time constants of the input stage.

The enabling technique not only reduces thermal errors but can reduce any "low frequency" aberration (thermal or electrical) in the transfer function of the comparator. The presence of undesirable electrical time constants (a linear systems phenomenon) within the comparator also can add tails to the settling performance. In either case, the problem is that the comparator's response time is too long. The enabling procedure for eliminating "thermal tails" also applies to these impulse response tails. In effect, the time difference, t_d, between the activation of the current source and the leading edge of the strobe, defines the effective response time of the comparator. Any tails in the impulse response of the comparator that extend beyond this duration will effectively be truncated. In the frequency domain, the frequency response of the comparator will be the Fourier transform of the truncated impulse response. The truncation will be manifested as a tendency to flatten the frequency response or transfer function for frequencies less than $1/t_d$. There is a practical limit, however, to reducing t_d to the point where short impulse tails cannot be truncated without causing other more serious response distortions.

Sampling Comparator Probe

Fig. 4 shows a simplified schematic of the probe circuit developed to evaluate the custom comparator. The comparator and associated devices and components are mounted on a multilayer board inside a palm-size metal case. The custom comparator chip is physically mounted within 2 mm of a type SMA input connector and 50 ohm termination. The direct mounting of the chip on the board, and its close proximity to the input, eliminates the parasitics contributed by the package lead-frame and minimizes the bond wire inductance. The quasi-static reference level from the A/D converter is buffered by a low-noise amplifier U1, the output of which is connected to the reference input of the comparator through a low-pass filter and 25 ohms of resistance. When using this comparator, it is

important for the high-frequency source resistances of each input to be nearly equal to obtain the fastest settling time of the first stage. A pair of ECL line drivers/receivers (U3 & U4), together with an RC network, provide the appropriate delay between the enable and strobe command to the comparator.

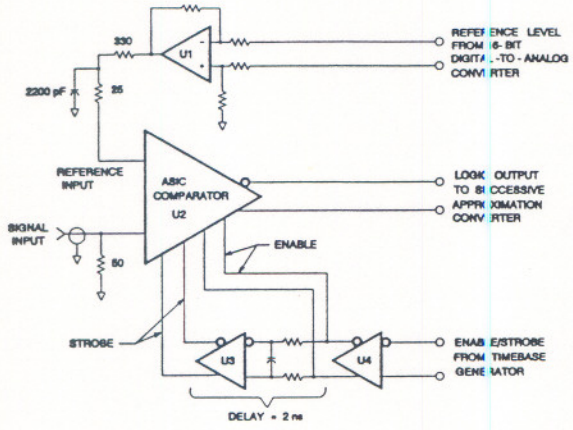

Fig. 4. Simplified schematic of the probe circuit for evaluating the custom comparator in a sampling comparator system.

PERFORMANCE RESULTS

The performance of the comparator was evaluated in the previously described probe circuit in conjunction with a commercial instrument that provides all of the necessary signals, display, and waveform processing. A preliminary summary of the salient features and characteristics of the comparator is listed below:

1) Transition Duration: (10-90%)	160 ps
2) Bandwidth: (from TD using 0.35/TD)	2.2 GHz
3) Settling Time: (referred to final DC value)	
to 0.1%	2 ns
to 0.02%	10 ns
4) Slew-rate limit:(above ±1 V)	5 V/ns
5) Input range:	±2.0 V
6) Maximum differential input	±4.0 V
7) Noise: (referred to the input)	320 μV RMS

Transition duration (TD) was measured by determining the time between the 10% and 90% amplitude points of the recorded response to a -0.25 V to 0 V, 16 ps TD step-like signal. Fig. 5 shows a plot of the sampled waveform from which the transition duration was determined. Settling time was determined by increasing the vertical sensitivity and noting the time required to settle to and remain within a given tolerence band from the mid-point of the transition. The measured transition duration exhibits some amplitude sensitivity. When the step amplitude is reduced to 0.125 V the reported duration increases to about 190 ps, indicating that the bandwidth is amplitude sensitive. The TD/amplitude effect levels out to about 220 ps at input levels below about 0.075 V. Similar results have been observed in most commercial comparators but to a much larger degree. This phenomenon is not well understood, but there is some indication that the response of the input stage to being overdriven, and the associated recovery may be responsible for this effect.

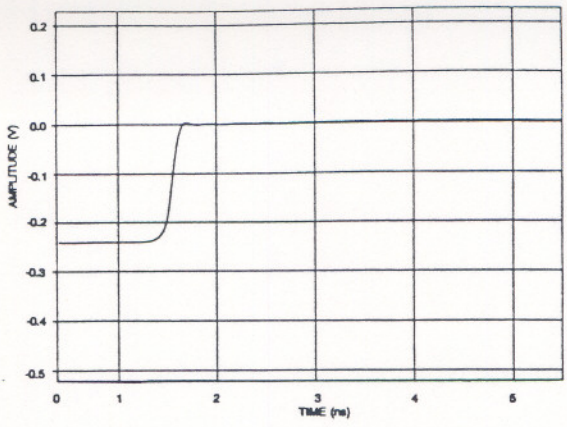

Fig. 5. Response to a 0.25 volt, 16 ps TD step generator.

Table 1
Harmonic Distortion

Frequency MHz	Input Level V rms	Largest Harmonic (2nd or 3rd) dB
1	0.1	-73
	1.0	-71
20	0.1	-76
	1.0	-63
50	0.05	-70
	1.0	-50
100	0.05	-56
	0.5	-44
	1.0	-40
200	0.5	-36
300	0.05	-46
	0.5	-36
	1.0	-30

Harmonic distortion was measured by recording a high-purity sine wave and using the processing capability of the commercial mainframe to determine the amplitude of the harmonics. Table 1 shows the measured values of harmonic distortion resulting from input signals from 1 to 300 MHz with amplitudes ranging from 50 mV to 1.0 V rms. The total harmonic distortion of the input signal, which was minimized by heavily filtering the output of a commercial generator, contributed an insignificant amount to these errors.

CONCLUSIONS

A custom integrated circuit comparator fabricated for high-performance sampling applications has been described. The comparator can be used in a sampling system for both frequency domain measurements, e.g. wideband rms voltage measurements, and high accuracy time domain pulse waveform measurements. The design has eliminated thermal effects common in other comparators that can cause errors and affect the voltage settling time. Elimination of thermal tail errors in the comparator coupled with its wide bandwidth provides an unsurpassed combination of speed and accuracy when used in equivalent-time sampling applications.

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