An Investigation of the Drive Circuit Requirements for the Power Insulated Gate Bipolar Transistor (IGBT)*

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***Abstract*—The drive circuit requirements of the IGBT are explained with the aid of an analytical model. It is shown that non-quasi-static effects limit the influence of the drive circuit on the time rate-of-change of anode voltage. Model results are compared with measured turn-on and turn-off waveforms for different drive, load, and feedback circuits and for different IGBT base lifetimes.**

I. Introduction

A SCHEMATIC of the structure of two of the many thousand cells of an n-channel IGBT (insulated gate bipolar transistor) is shown in Fig. 1. The IGBT functions as a bipolar transistor that is supplied base current by a MOSFET (Fig. 2), where the regions of each of these components are labeled on the right half of Fig. 1. The bipolar transistor of the IGBT consists of a low-doped wide base with the base virtual contact at the collector end of the base. This bipolar transistor has a low gain and is in the high-level injection condition for the practical current density range of the device. Consequently, the IGBT bipolar transistor cannot be described in traditional ways [1], [2]. The MOSFET portion of the IGBT behaves similarly to the structurally equivalent power VDMOSFET (Vertical doubled Diffused MOSFET), with the exception that the resistance of the lightly doped epitaxial layer is accounted for as the conductivity-modulated base resistance of the bipolar transistor.

It was shown in [3] that a newly developed non-quasi-static analytical model for the IGBT can be used to describe the output current and voltage turn-off switching waveform for general loading conditions. In this paper, the input and internal feedback capacitances similar to those for the structurally equivalent power MOSFET [4]–[7] are incorporated into the previously developed analytical IGBT bipolar transistor model of [1]–[3]. It is shown that this extended model can be used to describe the turn-on and turn-off, gate and anode, current and voltage waveforms for general external drive, load, and feedback circuits. The extended model is used to explain the influence of the drive circuit on the switching behavior and to examine different circuit configurations for active snubbing of the IGBT.

The effective output capacitance of the IGBT is much larger than the output capacitance of the structurally equivalent power MOSFET and this effective output capacitance varies with base lifetime [2]. This occurs because the excess carriers in the base are swept into a neutral base width that changes faster than the base transit speed during typical anode voltage transitions. It is shown in this paper that the additional component of output capacitance is coupled to the cathode and that the gate-drain feedback capacitance is unchanged from the value of a structurally equivalent power MOSFET. Because the IGBT output capacitance is much larger than the feedback capacitance and depends upon the instantaneous base charge, the relationship between the gate drive resistance and the time rate-of-change of anode voltage is significantly different for IGBT's than it is for the structurally equivalent power MOSFET.

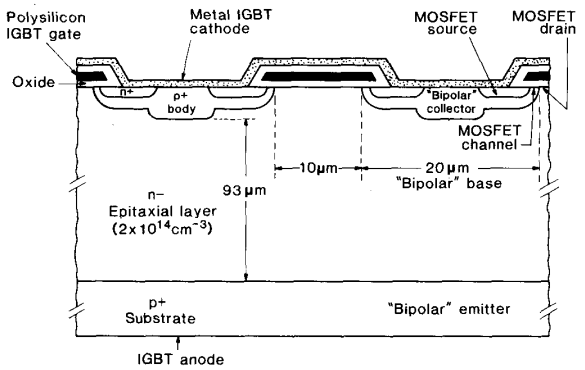

Fig. 1. Diagram of two diffused cells of n-channel IGBT.

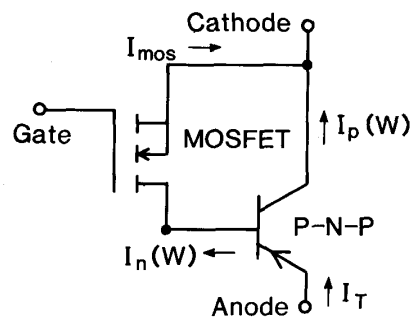

Fig. 2. Basic equivalent circuit model of IGBT.

II. IGBT Dynamic Model

In this section, an analytical model is presented that describes the dynamic behavior of the IGBT including the input characteristics and drive circuit dependence as well as the load circuit

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TABLE I
FUNCTIONS OF IGBT STATE VARIABLES

$$V_{ds} = V_{bc}$$
$$W_{gdj} = \sqrt{2\epsilon_{si}(V_{ds} - V_{gs} + V_{Td})/qN_B}$$
$$W_{dsj} = \sqrt{2\epsilon_{si}(V_{ds} + 0.6)/qN_B}$$
$$W_{bcj} = \sqrt{2\epsilon_{si}(V_{bc} + 0.6)/qN_B}$$
$$W = W_B - W_{bcj}$$
$$Q_B = qAWN_B$$
$$C_{bcj} \equiv A\epsilon_{si}/W_{bcj}$$
$$C_{dsj} = (A - A_{gd})\epsilon_{si}/W_{dsj}$$
$$C_{gdj} = A_{gd}\epsilon_{si}/W_{gdj}$$
$$C_{gd} = \begin{cases} C_{oxd} & \text{for } V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd} + C_{gdj}) & \text{for } V_{ds} > V_{gs} - V_{Td} \end{cases}$$
$$I_{mos} \approx \begin{cases} K_p(V_{gs} - V_T)V_{ds} - K_p\dfrac{V_{ds}^2}{2} & \text{for } V_{ds} \le V_{gs} - V_T \\ K_p(V_{gs} - V_T)^2/2 & \text{for } V_{ds} > V_{gs} - V_T \end{cases}$$

dependence. The IGBT model consists of three state equations that describe the evolution of the state of the base-collector voltage V_{bc}, the base charge Q, and the gate-source voltage V_{gs}. These state equations are expressed in terms of functions of the instantaneous values of the state variables, where the functions of the IGBT state variables are listed in Table I and the functions of the external circuit state variables, I_T and I_g, depend upon the external circuit configuration as described below.

MOSFET Input Characteristics

Fig. 3 shows the configuration of the MOSFET and bipolar equivalent circuit components superimposed on a schematic of one-half of the symmetric diffused IGBT cell. The MOSFET portion of the IGBT studied in this work behaves similarly to the power VDMOSFET, described in several recent publications [4]–[7], with the exception that the resistance of the lightly doped epitaxial layer is accounted for as the conductivity-modulated base resistance of the bipolar transistor, R_b. In addition, the drain-source and gate-drain depletion capacitances coincide with the base-collector depletion capacitance of the bipolar transistor and hence are only included in the MOSFET.

The expressions describing the equivalent circuit MOSFET of the IGBT's studied in this work are listed among the functions of the IGBT state variables in Table I. To describe IGBT's made with power MOSFET structures other than the VDMOSFET structure, the expressions in Table I can be replaced with the expressions for the appropriate structurally equivalent power MOSFET. The current through the MOSFET channel I_{mos} is well described by the expression in Table I for the 3-μm channel length IGBT's studied in this work [1]. Velocity saturation in the MOSFET channel [5], [7] is neglected in this paper for simplicity, but can be included for short channel lengths or high currents.

The dominant components of the VDMOSFET gate-source capacitance C_{gs} are due to the gate oxide capacitance of the source overlap C_{oxs} and due to the source metallization capacitance C_m indicated on Fig. 3. The dominant component of the MOSFET gate-drain capacitance C_{gd} is the gate oxide capacitance of the drain overlap C_{oxd} for $V_{ds} \le V_{gs} - V_{Td}$ or the series combination of the gate-drain overlap oxide capacitance and the gate-drain overlap depletion capacitance C_{gdj} for $V_{ds} > V_{gs} - V_{Td}$. The gate-to-channel and gate-to-body capacitances are neglected in this paper for simplicity [7].

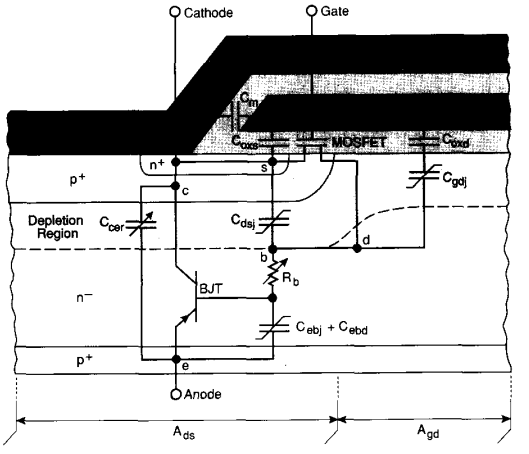

Fig. 3. Configuration of MOSFET and bipolar equivalent circuit components superimposed on schematic of one-half of symmetric IGBT cell.

The gate-drain overlap depletion capacitance C_{gdj} and the drain-source depletion capacitance C_{dsj} are voltage dependent due to the voltage dependencies of the respective depletion widths. The drain-source depletion width W_{dsj} is proportional to the square-root of the drain-source voltage plus the built-in potential of the junction ~ 0.6 V, and the gate-drain depletion width W_{gdj} is proportional to the square-root of the gate-drain voltage where the threshold voltage for the depletion of the epitaxial layer V_{Td} is approximately zero due to the low doping concentration of the epitaxial layer. The gate-drain capacitance is also proportional to the area of the gate-drain overlap A_{gd}, and the drain-source capacitance is proportional to the area of the body region A_{ds} (Fig. 3), where the sum of A_{gd} and A_{ds} is the active area of the chip A.

Bipolar Output Characteristics

The transient behavior of the lightly doped wide base bipolar transistor of the IGBT (and other conductivity-modulated devices) was analyzed in [2]. The transient carrier distribution and currents in the base are obtained by solving the ambipolar transport equations for the boundary conditions of the bipolar transistor. Fig. 4 shows the coordinate system used to develop the IGBT bipolar transistor model. Because the base-collector voltage changes with time during transient conditions, the base-collector depletion width changes with time, and the excess carrier charge stored in the base is swept into a neutral base width W that changes with time. It was shown in [1] that the base width changes faster than the base transit speed for excess carriers during typical IGBT transient operation; hence the ambipolar diffusion equation must be solved for the moving boundary condition to obtain the non-quasi-static transient carrier distribution and collector current.

As mentioned above, the base-collector depletion region coincides with the drain-source and gate-drain depletion regions. For the large values of base-collector voltage where the anode voltage changes rapidly during typical IGBT transient operation, the expressions for the depletion widths of the gate-drain overlap and the drain-source junction are approximately equal to each other, and equal to the expression for the effective base-collector junction depletion width W_{bcj} given in Table I. Using this expression for W_{bcj}, the time rate-of-change of base

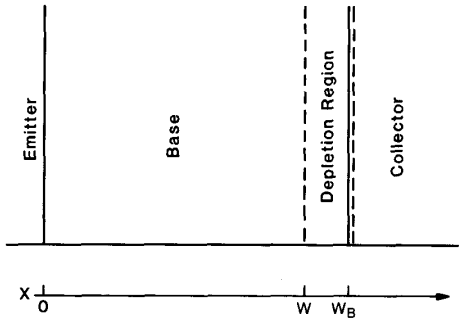

Fig. 4. Coordinate system used to develop IGBT bipolar transistor model. Emitter, base, and collector regions correspond to those indicated on right half of Fig. 1.

width W is given in terms of the time rate-of-change of base-collector voltage by

$$\frac{dW}{dt} = \frac{-C_{bcj}}{qN_BA} \cdot \frac{dV_{bc}}{dt}, \tag{1}$$

where $C_{bcj} \equiv A\epsilon_{si}/W_{bcj}$ is approximately equal to the sum of C_{gdj} and C_{dsj} for high base-collector voltages. It should be emphasized that C_{bcj} in (1) is used to describe the time rate-of-change of base width, but it not used to describe the displacement current through the base-collector junction depletion capacitance that is already accounted for by the sum of the drain-source and gate-drain capacitances.

The hole current at the collector edge of the neutral base (collector current of Fig. 2) for the moving boundary condition is given in [2] by

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right) \frac{4D_p}{W^2} Q + \frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B} \cdot \frac{dV_{bc}}{dt}, \tag{2}$$

where $b = \mu_n/\mu_p$. The first term on the right-hand side of (2) results from the coupling between the transports of electrons and holes for ambipolar transport, the second term is the well-known high-level injection charge control term, and the third term is a non-quasi-static term that is necessary to bring about the redistribution of carriers for the moving boundary condition. Because the third term is proportional to the time rate-of-change of base-collector voltage, it can be construed as a capacitive term where the capacitance is proportional to the instantaneous charge in the base Q [1]–[3]. This is indicated by the charge-dependent collector-emitter redistribution capacitance C_{cer} in Fig. 3.

IGBT State Equations

The expression for bipolar transistor collector current (2) was previously used to describe the IGBT turn-off transient for a rapid gate voltage transition where the MOSFET channel current is eliminated rapidly and the base current during turn-off is equal to the displacement current through the base-collector junction depletion capacitance. To include the drive circuit dependence, though, the electron current at the collector edge of the neutral base (base current of Fig. 2) is first expressed as the sum of the MOSFET channel current and the displacement currents through the drain-source and gate-drain capacitances:

$$I_n(W) = I_{mos} + (C_{dsj} + C_{gd}) \frac{dV_{ds}}{dt} - C_{gd} \frac{dV_{gs}}{dt}, \tag{3}$$

where I_{mos} is given in terms of the state variables of the IGBT (e.g., see Table I). Next, the gate current I_g is equated to the sum of the gate-source and gate-drain displacement currents, resulting in an expression for the time rate-of-change of the gate-source voltage:

$$\frac{dV_{gs}}{dt} = \frac{I_g}{C_{gs} + C_{gd}} + \frac{C_{gd}}{C_{gs} + C_{gd}} \cdot \frac{dV_{bc}}{dt}, \tag{4}$$

where $V_{ds} = V_{bc}$ has been used (see Fig. 3) and where the gate current is given in terms of the state variables of the external drive circuit as described below.

The state equation for the base-collector voltage is obtained by equating the total anode current I_T to the sum of the electron and hole components at $x = W$ ((2) and (3)), by substituting (4) for dV_{gs}/dt, and by then solving for the time rate-of-change of base-collector voltage:

$$\frac{dV_{bc}}{dt} = \frac{I_T - \frac{4D_p}{W^2} Q + \left(1 + \frac{1}{b}\right)\left[\frac{C_{gd}}{C_{gs} + C_{gd}} I_g - I_{mos}\right]}{\left(1 + \frac{1}{b}\right)\left[C_{dsj} + \frac{C_{gs}C_{gd}}{C_{gs} + C_{gd}} + \frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B}\right]}, \tag{5}$$

where $V_{ds} = V_{bc}$ has been used. In the model, the factor of $(1 + 1/b)$ is replaced by the expression $(1 + Q/b\{Q + Q_B\})$ so that this factor reduces to unity for low-level injection and to $(1 + 1/b)$ for high-level injection. Thus, (4) and (5) reduce to those for the structurally equivalent power MOSFET for $Q = 0$. The remaining IGBT state equation is obtained from the conservation of excess majority carrier base charge:

$$\frac{dQ}{dt} = I_{mos} + (C_{dsj} + C_{gd}) \frac{dV_{bc}}{dt} - C_{gd} \frac{dV_{gs}}{dt} - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2} I_{sne}, \tag{6}$$

where Q is supplied by the electron current at $x = W$ (3), and is depleted by recombination in the base (fourth term on the right-hand side of (6)) and by the injection of electrons into the emitter [1] (fifth term on the right-hand side of (6)).

To examine the behavior of the IGBT state equations, first consider the turn-off transient with a stiff gate drive circuit, so that V_{gs} is switched rapidly to its constant off-state value and (5) reduces to the state equation previously presented for this condition [1]–[3], by eliminating I_g between (4) and (5) and by then solving for dV_{bc}/dt where $C_{bcj} \approx C_{gd} + C_{dsj}$ is assumed. For this turn-off condition, the difference between the total current and the charge control component of collector current (first two terms in the numerator of (5)) is supplied by the current of the effective output capacitance C_{out} (denominator of (5)). As shown in [1]–[3], the moving boundary redistribution capacitance (last term in the brackets in the denominator of (5)) dominates the output capacitance and hence the voltage rate-of-rise at turn-off for the high-level injection condition that exists for typical IGBT transient operation. This occurs because the ratio of the excess carrier charge to the background mobile carrier

charge in the base Q/Q_B is much larger than unity for high-level injection.

Next, consider switching the IGBT with a small gate current so that the time rate-of-change of base-collector voltage is determined by the charging of the gate-drain feedback capacitance as described by (4). This occurs when the second term on the right-hand side of (4) cancels with the first term so that the time rate-of-change of gate-source voltage is reduced as the gate current charges the gate-drain feedback capacitance. The second term on the right-hand side of (4) can cancel with the first term during turn-off only if $I_g/C_{gd} < I_T/C_{\text{out}}$. For low-level injection or for the power VDMOSFET, C_{gdj} is on the same order of magnitude as C_{out} so the time rate-of-change of base-collector voltage is determined by the gate current if $I_g < I_T$. However, for high-level injection, the effective IGBT output capacitance is much larger than the gate-drain feedback capacitance, due to the moving boundary redistribution capacitance and a much smaller gate current is required to have an influence on the time rate-of-change base-collector voltage.

Conductivity-Modulated Base Resistance

The IGBT anode voltage is given by the sum of the bipolar transistor base-collector voltage and the emitter-base voltage (see Fig. 2):

$$V_A = V_{eb} + V_{bc}, \tag{7}$$

where the small series resistance due to the source wire bond and spreading resistance at its contact is neglected in this paper [1]. The emitter-base voltage was analyzed for the steady-state condition in [1]. Because V_{eb} is a small component of V_A during transient conditions, but is a significant component during the on-state, a quasi-static approach is used to include the steady-state emitter-base voltage expressions into the dynamic model. This gives a quantitative description for the steady-state and transient conditions and gives a qualitative description of the dynamic saturation effect discussed below [8].

The emitter-base voltage consists of three components as indicated in Fig. 3: the potential drop across the conductivity-modulated base resistance, the diffusion capacitance potential, and the depletion capacitance potential which is important for reverse blocking. For forward conduction, the steady-state emitter-base voltage was previously shown to be given by [1]:

$$V_{eb} = V_{ebd}(V_{bc}, Q) + I_T \cdot R_b(V_{bc}, Q), \tag{8}$$

where the conductivity-modulated base resistance R_b and the potential drop across the emitter-base diffusion capacitance V_{ebd} are obtained in terms of the instantaneous values of V_{bc} and Q from (10) and (11) of [3]. These expressions are formulated differently than those in [3] so that they describe the non-conductivity-modulated base resistance for low-level injection $Q < Q_B$, but for high-level injection they reduce to those in reference [3].

In the dynamic model, the expression for V_{eb} (8) depends upon the instantaneous values of both Q and I_T independently of one another. This becomes important for rapid turn-on conditions where the MOSFET portion of the device is switched on rapidly and the total load current I_T flows through the base before sufficient excess carrier charge Q is present to modulate the conductivity of the base. The emitter-base voltage at turn-on may be as large as the on-state voltage of the structurally equivalent power MOSFET, because Q is zero at the initiation of the turn-on and R_b is equal to the non-conductivity-modulated epitaxial layer resistance for $Q \ll Q_B$. However, Q rapidly approaches a value that is sufficient to modulate the resistance because the steady-state charge is typically several orders of magnitude larger than the background concentration.

The emitter-base junction depletion capacitance C_{ebj} indicated on Fig. 3 is important when the emitter-base junction is reverse biased or has a small forward bias, but for larger forward biases the emitter-base diffusion capacitance C_{ebd} is dominant. In the model, C_{ebj} is accounted for using the same state variable Q that accounts for C_{ebd}. For negative values of Q, the emitter-base junction is reverse biased (reverse blocking) and the state variable Q describes the space charge of the emitter-base depletion region. For this case, V_{eb} is given by the sum of the potential across the non-conductivity-modulated epitaxial layer resistance and the potential across the emitter-base junction depletion capacitance. In the model, a continuous transition between C_{ebj} ad C_{ebd} is imposed by using the larger of the two capacitances for small forward biases.

Interaction With External Circuits

To describe the interaction of the IGBT with the external drive, load, and feedback circuits, the state equations of the IGBT ((4)–(6) using Table I) are integrated simultaneously with the state equations of the external circuit where the expressions for I_T and I_g depend upon the external circuit configuration and where V_A is given in terms of the state variables by (7) and (8). The simultaneous integration of the state equations is performed using the readily available RKF45 subroutine [9] in a FORTRAN program where the initial conditions are used for a known steady-state condition. The RKF45 subroutine uses an automatic Runge–Kutta–Fehlberg method to iteratively evaluate a user-defined subroutine that contains the state equations of the IGBT and the state equations of the external circuit. The FORTRAN program is called INSTANT (IGBT Network Simulation and Transient Analysis Tool) and simulates the dynamic behavior of multiple IGBT's in any external drive, load, and feedback circuit configuration [10], [11].

As an example, consider the dynamic behavior of the IGBT for the series resistor-inductor load circuit and the resistive drive circuit shown in Fig. 5. The load circuit state equation for the circuit of Fig. 5 is

$$\frac{dI_L}{dt} = \frac{1}{L_L}(V_{AA} - R_L I_L - V_A), \tag{9}$$

where $I_T = I_L$ for this load. The gate current for the circuit of Fig. 5 is given by

$$I_g = (V_{gg} - V_{gs})/R_g, \tag{10a}$$

where the gate pulse generator voltage is given by

$$V_{gg} = \begin{cases} 0 & \text{for } t \le t_{\text{on}} \\ V_{g\text{on}} & \text{for } t_{\text{on}} < t < t_{\text{off}} \\ 0 & \text{for } t \ge t_{\text{off}} \end{cases}. \tag{10b}$$

The pulse generator rise and fall times are also included in the simulations below but are not indicated in (10b) for simplicity. The initial conditions of the state variables before the initiation of the gate pulse are $V_{gs} = 0$, $Q = 0$, $V_{bc} = V_{AA}$, and $I_L = 0$. To simulate the dynamic operation of the IGBT in different circuits, only the circuit state equations need to be changed. The IGBT model itself is contained within two subroutines to simplify the implementation of different circuits [10], [11]; the first

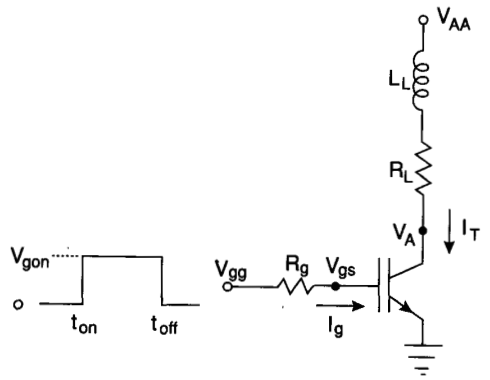

Fig. 5. Circuit configuration of IGBT with series resistor-inductor load and resistive gate drive.

subroutine evaluates the emitter-base junction voltage and the conductivity-modulated base resistance (8), and the second subroutine evaluates the IGBT state equations ((4)–(6) and Table I).

Other second-order effects that are incorporated into the IGBT model but are not described in detail in this paper are: mobility reduction due to high free carrier levels, velocity saturation in the base-collector depletion region, and carrier multiplication within the base-collector depletion region. The mobility reduction due to high free carrier levels has a second-order effect upon the on-state emitter-base voltage and is implemented iteratively within the emitter-base voltage subroutine [1]. The space charge concentration due to the velocity saturation within the base-collector depletion region has a second-order effect on the time rate-of-change of the base-collector voltage and is implemented iteratively within the IGBT state equation subroutine. Carrier multiplication within the base-collector depletion region results in additional components of collector and base currents that increase exponentially with anode voltage near the open-base, collector-emitter breakdown voltage. The carrier multiplication is included in the derivation of the IGBT state equations by including additional components of base current in (3) that are proportional to the electron and hole currents entering the depletion region, $I_p(W)$ and I_{mos}, and that are proportional to the multiplication factor $(M-1)$ [12].

III. Comparison of Theory and Experiment

In this section, the predictions of the theoretical model described in the last section are compared with experimental results for IGBT's with the parameters listed in Tables II and III and for devices with different base lifetimes (an exception to Table II is that the base width of the 0.3-μs device is 110 μm). The simulations and measurements are made for load circuit parameters similar to those used in reference [3], but for gate drive resistances that range from 10 Ω through 10 kΩ. It is shown in this section that the gate drive resistance does not influence the anode voltage rate-of-rise at turn-off for gate resistances smaller than 1 kΩ for the 7.1-μs device, 500 Ω for the 2.5-μs device, and 25 Ω for the 0.3-μs device, whereas the voltage rate-of-rise at turn-off is influenced by resistances as low as 2 Ω for the structurally equivalent power MOSFET. However, the turn-on speed is as rapid as that of the structurally equivalent power MOSFET for all of the different base lifetime IGBT's and is limited by the dynamic saturation effect. Thus, the gate drive requirements of the IGBT are inherently asymmetrical and the degree of asymmetry depends upon the device base lifetime. This is consistent with the data summary in Table I of [13].

TABLE II
Device Parameters

N_B	2×10^{14} cm^{-3}
A	0.1 cm^2
W_B	93 μm
I_{sne}	6.0×10^{-14} A
K_p	0.36 A/V^2
V_T	5.0 V
A_{gd}	0.05 cm^2
C_{oxd}	1.6 nF
C_{gs}	0.6 nF
V_{Td}	~0 V

TABLE III
Physical Constants at SI at T = 25°C

n_i	1.45×10^{10} cm^{-3}
μ_n	1500 cm^2/V − s
μ_p	450 cm^2/V − s
ϵ_{si}	1.05×10^{-12} F/cm

Extraction Of MOSFET Dynamic Parameters

The first six parameters listed in Table II were extracted as described in [1] and [11]. The remaining four model parameters describe the IGBT dynamic input and internal feedback characteristics and are extracted from turn-on gate and anode voltage waveforms for a nearly constant gate current and for a load that results in a low anode current, R_L = 1 kΩ through 10 kΩ. For the low anode current, Q = 0 and the gate charging characteristics are similar to those of the structurally equivalent power MOSFET [4]–[7], with the exception of the addition of the emitter-base junction capacitance. The nearly constant gate current pulse $I_g \sim 20$ mA is obtained by using a large gate voltage pulse amplitude V_{gon} = 100 V and a large gate resistance R_g = 5 kΩ, where a short gate current pulse width <2 μs is used to prevent the gate voltage from exceeding its rated maximum value.

The measured IGBT gate charging characteristics for V_{AA} = 20 V are shown in Fig. 6(a) and those for V_{AA} = 300 V are shown in Fig. 6(b). The gate voltage waveforms consist of three phases as indicated on Fig. 6(a). During the first phase, V_{gs} rises with a constant slope as the constant gate current charges the constant gate-source capacitance and the small high voltage gate-drain depletion capacitance. During the second phase, V_{gs} remains virtually constant and V_A falls as the gate current charges the voltage-dependent gate-drain feedback capacitance. The gate voltage remains virtually constant because only a small increase of V_{gs} above V_T is necessary for the MOSFET channel to supply the small load current and the small output capacitance displacement current. Fig. 6(a) emphasizes the range of V_A for which C_{gd} is equal to the gate-drain overlap oxide capacitance $V_{ds} < V_{gs} - V_{Td}$, and Fig. 6(b) emphasizes the range for which C_{gd} is inversely proportional to the square-root of the gate-drain voltage. During the third phase of the gate voltage waveform, V_A remains relatively constant at its on-state value and V_{gs} rises with a constant slope (different slope than that during the first phase) as the gate current charges the sum of the gate-drain overlap oxide capacitance and the gate-source capacitance.

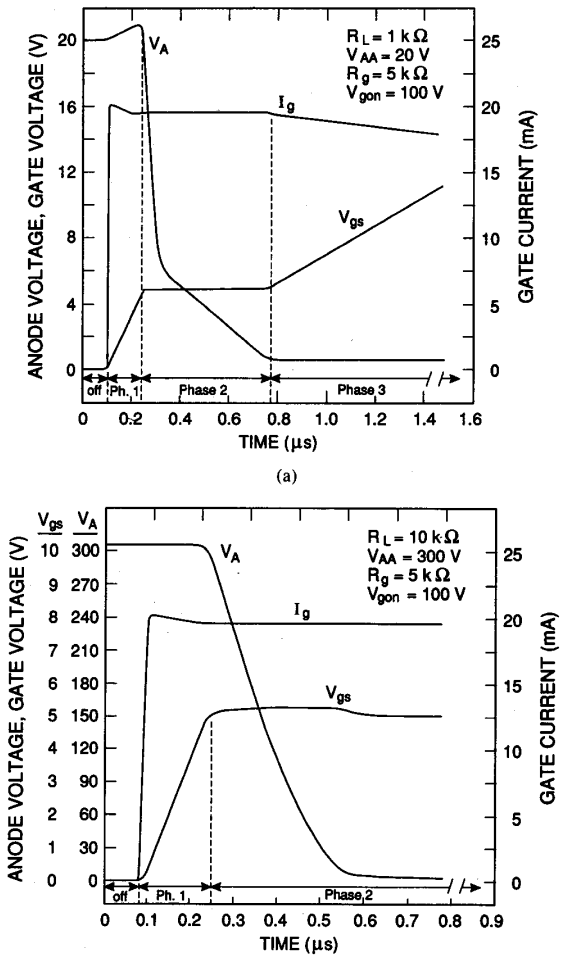

Fig. 6. Measured gate charging characteristics for low anode current and relatively constant ~20 mA gate current pulse where (a) is for V_{AA} = 20 V and (b) is for V_{AA} = 300 V.

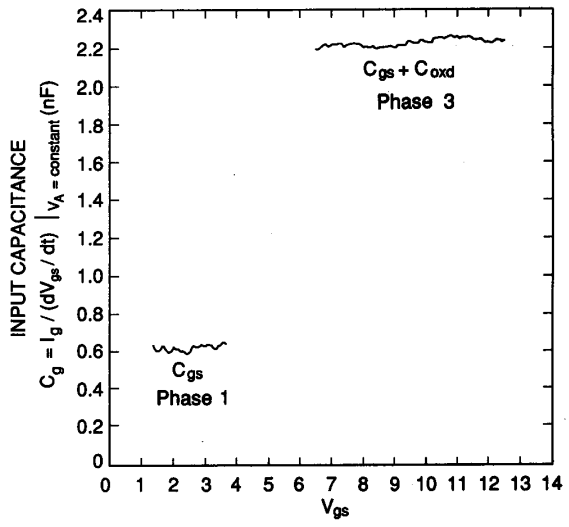

Fig. 7. Measured input capacitance versus gate voltage characteristics for V_{AA} = 300 V obtained from digitized gate current and gate voltage waveforms similar to those in Fig. 6.

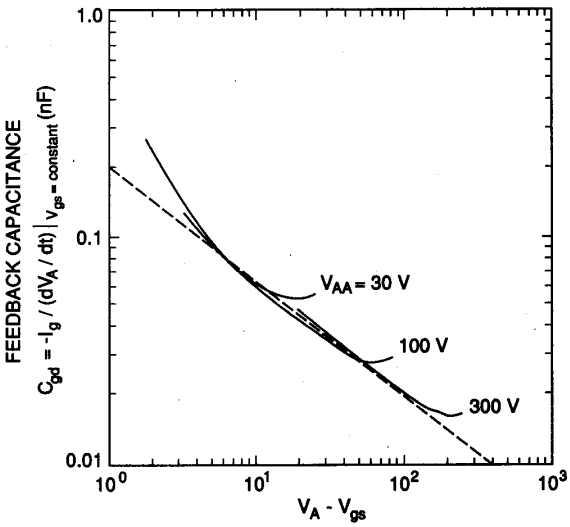

Fig. 8. Measured gate-drain feedback capacitance versus anode-gate voltage obtained from digitized gate current, gate voltage, and anode voltage waveforms similar to those in Fig. 6 for anode supply voltages of 30 V, 100 V, and 300 V.

Fig. 7 shows the measured input capacitance versus gate-source voltage for V_{AA} = 300 V. These characteristics are obtained from the first and third phases of the measured turn-on waveforms by dividing the digitized gate current waveform by the time rate-of-change of gate voltage. The time rate-of-change of gate voltage is obtained numerically from the digitized gate voltage waveform. Because the gate-drain capacitance at V_A = 300 V is much smaller than the gate-source capacitance, the input capacitance during the first phase is used to extract the value of C_{gs} in Table II. Because the gate-drain voltage is larger than V_{Td} during the third phase, the input capacitance during the third phase is equal to the sum of the gate-source capacitance and gate-drain overlap oxide capacitance. Thus, the value of C_{oxd} in Table II is extracted by subtracting the value of the input capacitance during the first phase from that during the third phase.

Fig. 8 shows the measured gate-drain feedback capacitance versus anode-gate voltage obtained from three different values of V_{AA}. These characteristics are obtained from the second phase of the measured turn-on waveforms by dividing the digitized gate current waveform by the time rate-of-change of anode voltage. The time rate-of-change of anode voltage is obtained numerically from the digitized anode voltage waveform, and the anode-gate voltage is obtained by subtracting the gate voltage waveform from the anode voltage waveform. For $V_{ds} >> V_{gs} - V_{Td}$, the gate-drain capacitance is inversely proportional to the square-root of the gate-drain voltage because $C_{gdj} << C_{oxd}$ (Table I). This is evidenced by the slope of negative one-half on the log-log plot of Fig. 8 (dashed line). The deviation from this slope at low anode voltages is primarily due to the emitter-base voltage offset (7) and hence the offset due to V_{Td} is approximately zero. The value of A_{gd} in Table II is extracted form

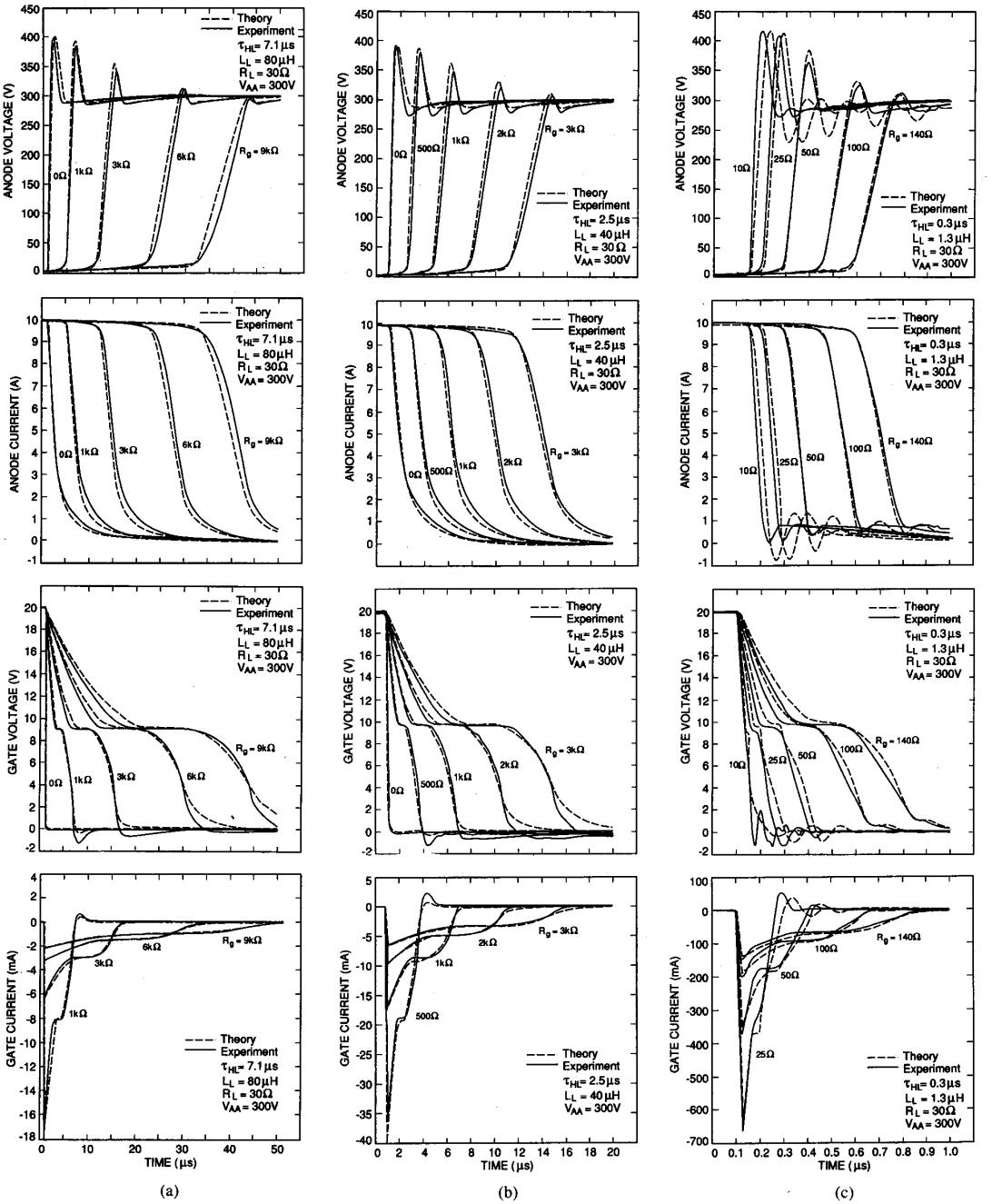

Fig. 9. Comparison of measured and simulated, gate and anode, current and voltage turn-off waveforms for the circuit of Fig. 5 with different values of gate resistance, where (a) is for 7.1-μs device, (b) is for 2.5-μs device, and (c) is for 0.3-μs device.

the expression for C_{gdj} in Table I by fitting the line with slope of negative one-half (dashed line in Fig. 8) to the high voltage gate-drain capacitance data. For $V_{ds} < V_{gs} - V_{Td}$, the gate-drain capacitance is constant as is evident from Fig. 6(a) and C_{oxd} can also be extracted from the second phase of the turn-on waveforms.

Turn-Off Transient

Fig. 9(a)–(c) show the measured and simulated, gate and anode, current and voltage turn-off waveforms for the circuit of Fig. 5 with different values of gate resistance, where Fig. 9(a)–(c) are each for a diferent device base lifetime and load inductance. The load inductances are chosen for each device so that

the anode voltage overshoot will not exceed the device voltage rating of 500 V [3]. The simulations are performed as described in Section II using the parameters in Tables II and III. The gate voltage pulse amplitude of $V_{g\,on} = 20$ V is chosen so that the plateau in gate current occurs at approximately the same magnitude for turn-on as for turn-off. The 15-ns fall time of the gate pulse generator is also included in the simulations. The gate voltage pulse widths for the simulations and measurements are chosen so that a steady-state condition is reached before the devices are switched off. The load resistance of 30 Ω results in a steady-state current of 10 A for the anode supply voltage of 300 V.

The turn-off sequence of Fig. 9(a)–(c) begins when V_{gg} is switched rapidly to zero. Initially, V_{gs} begins to fall as the gate capacitance is discharged through the gate resistance, and V_{ds} rises a few volts so that the current through the MOSFET channel (linear region of I_{mos} in Table I) remains relatively constant. Once V_{gs} has fallen and V_{ds} has risen to the point where the MOSFET enters the current saturation region $V_{ds} \geq V_{gs} - V_T$, the gate voltage remains constant at $V_{gs} = V_T + \sqrt{2I_{mos}/K_P}$ and the gate current charges the large gate-drain overlap oxide capacitance as V_{ds} rises slightly faster. This plateau in V_{gs} continues until V_{ds} rises to the point where the gate-drain overlap capacitance becomes depleted, $V_{ds} \geq V_{gs} - V_{Td}$. Beyond this point, the gate-drain feedback capacitance is reduced by about two orders of magnitude and the anode voltage rate-of-rise increases sharply. Because V_A rises only slightly during the first two phases (from the on-state voltage to about 10 V), they are perceived as a delay in the turn-off where the delay time is nearly proportional to the gate resistance.

After the turn-off delay, the anode voltage rate-of-rise is determined by the effective output capacitance C_{out} (denominator of (5)) if $I_g/C_{gdj} \gg I_T/C_{\text{out}}$; otherwise, the anode voltage rate-of-rise is limited by the gate current that charges the high-voltage gate-drain feedback capacitance C_{gdj} as described in the discussion of (4) and (5). For a power MOSFET with a structure similar to that of the IGBT in Fig. 1, C_{out} is on the same order of magnitude as C_{gdj} because $A_{gd} \approx A_{ds}$ and the gate current limits the anode voltage rate-of-rise for $I_g < I_T$, i.e., for $R_g > 2\ \Omega$. However, as mentioned above, the effective output capacitance of the IGBT is several orders of magnitude larger than that of the structurally equivalent power MOSFET and depends upon the device base lifetime. Thus, the rate-of-rise of anode voltage and the anode voltage overshoot are not affected by gate resistances below 1 kΩ for the 7.1-μs IGBT of Fig. 9(a), below 500 Ω for the 2.5-μs IGBT of Fig. 9(b), or below 25 Ω for the 0.3-μs IGBT of Fig. 9(c). For gate resistances larger than these values, though, the anode voltage rate-of-rise and the voltage overshoot are reduced (active snubbing).

Turn-On Transient

Fig. 10 shows the measured and simulated, gate and anode, current and voltage turn-on waveforms for the circuit of Fig. 5 with different values of gate resistance. The disagreement between the simulated and measured gate current and gate voltage waveforms is due to the source lead inductance which is not included in the simulations for simplicity. The small value of load inductances is chosen for this example to show that both the anode current and anode voltage can change rapidly at turn-on. Because the turn-on waveforms are relatively independent of device base lifetime, they are only shown for the 2.5-μs device. The simulations are performed as described in Section II

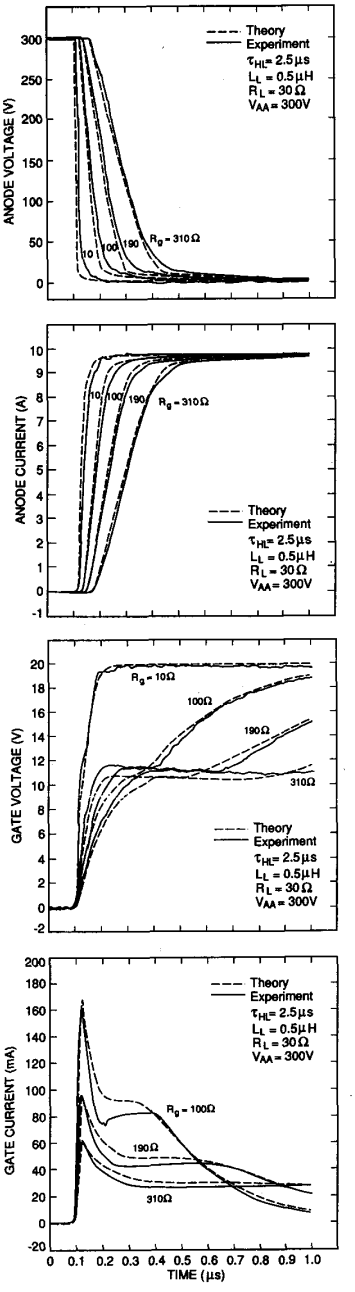

Fig. 10. Comparison of measured and simulated, gate and anode, current and voltage turn-on waveforms for circuit of Fig. 5 with different values of gate resistance.

using the parameters in Tables II and III. The gate voltage pulse amplitude of $V_{g\,on} = 20$ V is the same as for the turn-off results and the rise time of the gate pulse generator is also 15 ns.

The turn-on sequence of Fig. 10 begins when V_{gg} is switched rapidly to $V_{g\,on}$. Initially, V_{gs} rises as the gate capacitance is charged through the gate resistance and V_A remains relatively constant at V_{AA} while $V_{gs} < V_T$. This phase appears as a short turn-on delay that is proportional to the gate resistance. Once

V_{gs} exceeds V_T, the MOSFET enters its saturation region and the anode current increases as V_{gs} continues to increase. During this phase, the gate current charges the gate-source capacitance and discharges the gate-drain capacitance as V_A decreases rapidly. Once V_{gs} has risen and V_{ds} has fallen to the point where the gate-drain overlap depletion region vanishes, $V_{ds} \leq V_{gs} - V_{Td}$, the gate-drain capacitance increases by approximately two orders of magnitude, so V_{gs} remains relatively constant at $V_{gs} = V_T + \sqrt{2I_{mos}/K_p}$ and the gate current charges the large gate-drain overlap oxide capacitance as V_A falls slowly. Once V_{ds} is reduced to the point where the MOSFET enters the linear region $V_{ds} \leq V_{gs} - V_T$, the gate voltage begins to rise again and V_{ds} continues to fall slowly so that the current through the MOSFET channel (linear region of I_{mos} in Table I) remains relatively constant.

Comparing Figs. 9 and 10, it is evident that the anode voltage rate-of-fall at turn-on is influenced by much smaller gate resistances than those that influence the anode voltage rate-of-rise at turn-off. This occurs because Q is zero at the beginning of the turn-on sequence and the effective output capacitance depends upon Q (denominator of (5)). Thus, the anode voltage rate-of-fall at turn-on is as rapid for the IGBT as it is for the structurally equivalent power MOSFET. The speed of the low anode voltage portion of the IGBT turn-on waveform (lower than the MOSFET on-state voltage) is limited, though, for $R_g < 30\ \Omega$ by the finite time required to supply the base charge that modulates the base resistance (dynamic saturation). For $R_g > 30\ \Omega$, the turn-on speed at low anode voltages is limited by the time required for the gate current to discharge the gate-drain overlap oxide capacitance.

Fig. 11 shows the instantaneous emitter-base voltage and base charge for the same turn-on conditions as the $R_g = 10\ \Omega$ waveform of Fig. 10 and for two different device base lifetimes. For small load inductances and small gate resistances, the anode current can rise much faster than the base charge so that the base resistance is not conductivity-modulated and the emitter-base voltage may initially be as large as that for the structurally equivalent power MOSFET ~ 15 V. But, the base resistance rapidly becomes modulated, because I_{mos} is initially nearly as large as the total current ~ 10 A and thus Q approaches ten times the background base charge ($Q_B \sim 30\ nC$) in approximately 30 ns (see (6) and the time rate-of-change of Q on Fig. 11). The turn-on speed is relatively independent of the device base lifetime because the time required to modulate the base resistance depends primarily upon the MOSFET current and the base transit time.

Active Snubbing

It has been proposed by others (e.g., [14]) that the gate resistance can be used to control the voltage rate-of-rise at turn-off for the IGBT (active snubbing). However, as can be seen from Fig. 9, a large value of gate resistance is required to have an influence on the voltage rate-of-rise at turn-off for the IGBT's. Therefore, it is beneficial to use a polarized gate drive resistance in this instance so that the turn-on time is not also increased. In addition, a very long, possibly unacceptable turn-off delay time results for gate resistances large enough to have an influence on the IGBT anode voltage rate-of-rise at turn-off (e.g., 30-μs turn-off delay for the $R_g = 9\ k\Omega$ waveform in Fig. 9(a)). This occurs because the gate-drain overlap oxide capacitance is much larger than the high voltage gate-drain overlap depletion capacitance.

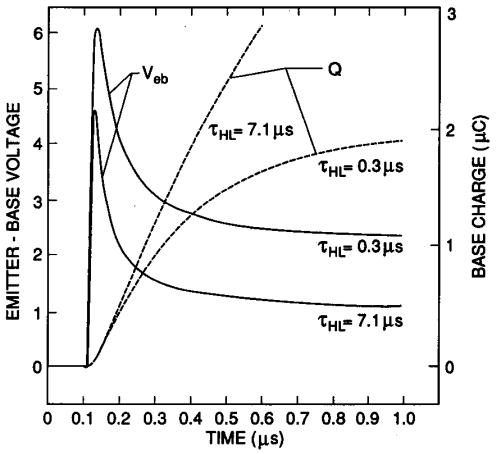

Fig. 11. Emitter-base voltage and base charge for same turn-on conditions as $R_g = 10\ \Omega$ waveform of Fig. 10 and for two different device base lifetimes.

It has been suggested by others [15], though, that the time rate-of-change of drain voltage for power VDMOSFET's can be controlled independently of the delay time by inserting a small capacitor from gate-to-drain. This occurs because the ratio of the net gate-to-drain feedback capacitance at high voltages to that at low voltages is increased by inserting the external feedback capacitor. This technique is especially beneficial for the IGBT due to the excessively long delay times incurred. It is also proposed here, that a large gate-to-anode feedback resistor be placed in series with the external gate-to-anode feedback capacitor when used with the polarized gate resistance, so that the turn-on speed is not significantly reduced by the feedback network for a given turn-on gate resistance. A minimal value of series feedback resistance is also necessary to suppress high frequency oscillations [16].

Fig. 12 shows the circuit configuration for the IGBT with a series resistor-inductor load, a polarized gate drive resistance, and a series resistor-capacitor external feedback circuit. To simulate the operation of this circuit, an additional state equation for the potential across the external feedback capacitor V_{cf} is necessary:

$$\frac{dV_{cf}}{dt} = \frac{I_f}{C_f}, \tag{11}$$

where the feedback current is given by

$$I_f = (V_A - V_{cf} - V_{gs})/R_f. \tag{12}$$

For this circuit, the IGBT anode current is given by $I_T = I_L - I_f$, and the anode voltage is obtained in terms of the state variables by combining this expression with (7), (8), and (12). The expression for the gate current (10a) is replaced by

$$I_g = \begin{cases} I_f + (V_{gg} - V_{gs})/R_g, & \text{for } V_{gg} < V_{gs} + 0.7\ \text{V} \\ I_f + (V_{gg} - V_{gs})/R_g + (V_{gg} - V_{gs} - 0.7)/R_{gon}, & \text{for } V_{gg} \geq V_{gs} + 0.7\ \text{V} \end{cases} \tag{13}$$

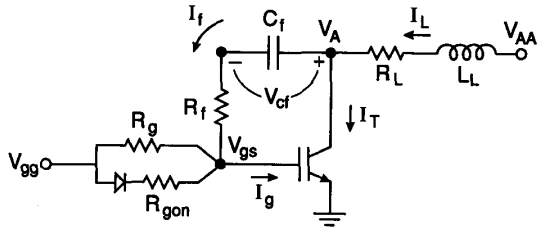

Fig. 12. Circuit configuration of IGBT with series resistor-inductor load, polarized gate drive resistance, and series resistor-capacitor feedback circuit.

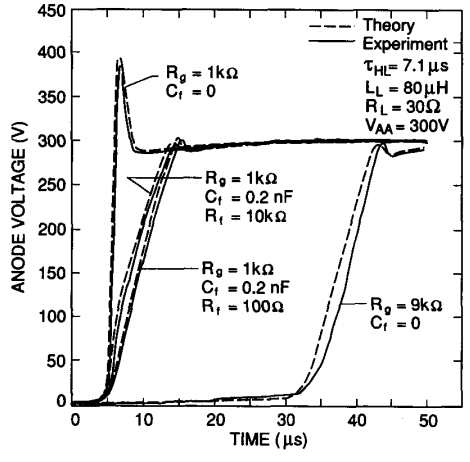

Fig. 13. Comparison of measured and simulated anode voltage turn-off waveforms for the circuit of Fig. 12 with different values of gate resistance, external gate-to-anode feedback capacitances, and different series feedback resistances.

where the diode is modeled as a 0.7-V offset and a 1-Ω effective series resistance that is included in $R_{g\,on}$. The initial condition for the feedback capacitor voltage before the initiation of the gate voltage pulse is $V_{cf} = V_{AA}$.

As an example, Fig. 13 compares the simulated and measured turn-off anode voltage waveforms for circuit conditions similar to those of Fig. 9(a) with the exception that the external feedback circuit components of Fig. 12 are included in two of the waveforms. The R_g = 1-kΩ and 9-kΩ waveforms of Fig. 9(a) (i.e., $C_f = 0$) are repeated on Fig. 13 for comparison. It is evident from this figure that if a 0.2-nF external gate-to-anode capacitor is inserted, the 1-kΩ gate resistor results in a time rate-of-change of anode voltage and voltage overshoot similar to the 9-kΩ waveform of Fig. 9(a), but with a turn-off delay similar to that of the 1-kΩ waveform of Fig. 9(a). It is also evident from Fig. 13 that values of series feedback resistance as large as R_f = 10 kΩ do not diminish the effect of the feedback capacitor for the 1-kΩ gate resistor.

However, the effect of the feedback capacitor at turn-on is diminished by a series feedback resistance of 10 kΩ, because the turn-on gate current is larger than the turn-off gate current for the polarized gate resistance, and the feedback current becomes negligible if V_A/R_f is much less than the gate current. For example, Fig. 14 compares the simulated and measured

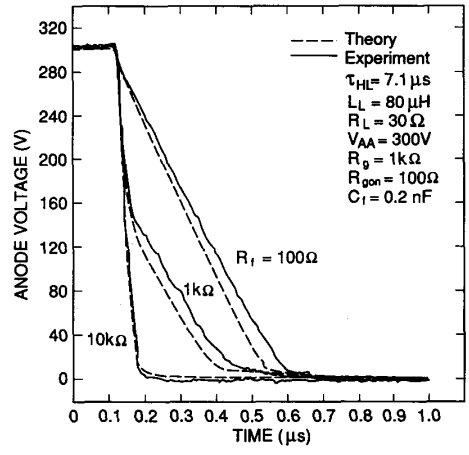

Fig. 14. Comparison of measured and simulated, anode voltage turn-on waveforms for circuit of Fig. 12 with different values of series feedback resistances.

turn-on anode voltage waveforms for the same circuit conditions as for Fig. 13 and for a turn-on gate resistance of $R_{g\,on}$ = 100 Ω. For $R_f \leq$ 100 Ω, the anode voltage rate-of-fall is determined by the gate current charging the external gate-to-anode feedback capacitor. However, for $R_f \geq$ 10 kΩ, the turn-on anode voltage waveform is similar to the R_g = 100 Ω waveform of Fig. 10 (i.e., $C_f = 0$). Thus, the rate-of-rise of anode voltage at turn-off is controlled independently of the turn-off delay time and independently of the rate-of-fall of anode voltage at turn-on without increasing the drive circuit current requirements; i.e., it is not necessary to reduce $R_{g\,on}$ to compensate for the addition of the external gate-to-anode feedback capacitor.

IV. Conclusion

An analytical model is developed for the IGBT that can be used to describe the turn-on and turn-off, gate and anode, current and voltage waveforms for general external drive, load, and feedback circuits. The IGBT model incorporates the input and internal feedback capacitance of the structurally equivalent power MOSFET into the previously developed non-quasi-static model for the IGBT bipolar transistor output characteristics. The bipolar transistor model includes the charge-dependent non-quasi-static collector-emitter redistribution capacitance that is important for the IGBT because the neutral base width changes faster than the base transit speed for excess carriers during typical IGBT transient operation. The bipolar transistor model also includes the charge-dependent conductivity-modulated base resistance independently of the device current, and thus describes the dynamic saturation of base-emitter voltage due to the finite time required to supply the base charge that modulates the conductivity of the base.

The effective output capacitance of the IGBT at turn-off is several orders of magnitude larger than that of the structurally equivalent power MOSFET and depends upon the device base lifetime because the base charge at turn-off depends upon the device base lifetime. However, the gate-drain feedback capacitance is unchanged from the value for the structurally equiva-

lent power MOSFET. Thus, the minimum gate resistance that influences the anode voltage rate-of-rise at turn-off is several orders of magnitude larger than that for the power MOSFET and varies with device base lifetime. Because the base charge is zero at the initiation of turn-on, the IGBT output capacitance is much smaller at turn-on than at turn-off and the anode voltage rate-of-fall at turn-on is influenced by gate resistance as small as those that influence the structurally equivalent power MOSFET. The IGBT turn-on speed is limited at low anode voltages, though, by the time required to supply the charge that modulates the conductivity of the base and is relatively independent of device base lifetime.

The IGBT gate drive requirements are inherently asymmetrical, and the degree of asymmetry depends upon the device base lifetime. Therefore, it is beneficial to use a polarized gate drive resistance for the IGBT. Because the turn-off delay time is excessively long for gate resistances large enough to control the IGBT voltage rate-of-rise at turn-off, it is beneficial to insert an external anode-to-gate feedback capacitor so that the anode voltage rate-of-rise at turn-off is controlled independently of the turn-off delay. It is also beneficial to insert a large resistance in series with the external feedback capacitor when used with the polarized gate drive resistance, so that the turn-on speed is not influenced by the feedback capacitor. Thus, the anode voltage rate-of-rise at turn-off can be controlled independently of the turn-off delay time and independently of the anode voltage rate-of-fall at turn-on, without increasing the current capability of the drive circuit for turn-on.

NOMENCLATURE

A	Device active area (cm^2).
A_{ds}	Body region area (cm^2).
A_{gd}	Gate-drain overlap area (cm^2).
$b = \mu_n/\mu_p$	Ambipolar mobility ratio.
C_{bcj}	Base-collector depletion capacitance (F).
C_{dsj}	Drain-source depletion capacitance (F).
C_{ebj}	Emitter-base depletion capacitance (F).
C_{ebd}	Emitter-base diffusion capacitance (F).
C_f	External feedback capacitor (F).
C_{gd}	Gate-drain capacitance (F).
C_{gdj}	Gate-drain overlap depletion capacitance (F).
C_{gs}	Gate-source capacitance (F).
C_{out}	Effective output capacitance (F).
C_{oxd}	Gate-drain overlap oxide capacitance (F).
D_n, D_p	Electron, hole diffusivity (cm^2/s).
I_f	Feedback current (A).
I_g	Gate current (A).
I_L	Load inductor current (A).
I_{mos}	MOSFET channel current (A).
I_n, I_p	Electron, hole current (A).
I_{sne}	Emitter electron saturation current (A).
I_T	Anode current (A).
K_p	MOSFET transconductance parameter (A/V^2).
L_L	Series load inductance (H).
n_i	Intrinsic carrier concentration (cm^{-3}).
N_B	Base doping concentration (cm^{-3}).
q	Electronic charge (1.6×10^{-19} C).
Q	Instantaneous excess carrier base charge (C).
Q_B	Background mobile carrier base charge (C).
R_b	Conductivity modulated base resistance (Ω).
R_f	Series feedback resistance (Ω).
R_g	Gate drive resistance (Ω).
$R_{g\,\text{on}}$	Turn-on gate resistance (Ω).
R_L	Series load resistance (Ω).
V_A	Device anode voltage (V).
V_{AA}	Anode supply voltage (V).
V_{bc}	Applied base-collector voltage (V).
V_{cf}	External feedback capacitor voltage (V).
V_{ds}	Applied drain-source voltage (V).
V_{eb}	Applied emitter-base voltage (V).
V_{ebd}	Emitter-base diffusion potential (V).
V_{gg}	Gate pulse generator voltage (V).
$V_{g\,\text{on}}$	Gate pulse voltage amplitude (V).
V_{gs}	Gate-source voltage (V).
V_T	MOSFET channel threshold voltage (V).
V_{Td}	Gate-drain overlap depletion threshold (V).
W	Quasi-neutral base width (cm).
W_B	Metallurgical base width (cm).
W_{bcj}	Base-collector depletion width (cm).
W_{dsj}	Drain-source depletion width (cm).
W_{gdj}	Gate-drain overlap depletion width (cm).
x	Distance in base from emitter (cm).
ϵ_{si}	Dielectric constant of silicon (F/cm).
μ_n, μ_p	Electron, hole mobility ($cm^2/V - s$).
τ_{HL}	Base high-level lifetime (s).

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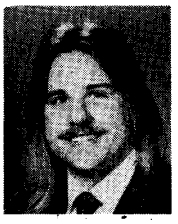

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