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The Fabrication of Thin, Freestanding, Single-Crystal, Semiconductor Membranes

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ABSTRACT

Freestanding, single-crystal, semiconductor membranes with thicknesses in the range of a few tens of nanometers to tens of microns are of increasing technological interest today. Their applications range from high speed electronic devices to electromechanical devices and pressure sensors. This review paper identifies two general classes of techniques for producing such thin membranes: dissolution of single-crystal wafers, and direct growth of single-crystal membranes. Numerous specific techniques in each general class are discussed. The discussion of each technique includes a brief explanation of the reason why it works, a description of the actual experimental implementation, an analysis of the range of thickness that can be produced, and the crystalline and electrical quality of the membranes. Unusual difficulties with implementing a technique, or special advantages of a technique are also noted. Since this review is intended to aid in the selection of a technique for producing thin semiconductor membranes when one has a particular application in mind, note is made of those applications for which the membranes produced with each technique are particularly well suited.

The need for self-supported thin single-crystal semiconductor membranes.—There has been a great interest for many years in thin, self-supporting, single-crystal, device quality semiconductor membranes. The first interest in such membranes dates back to the 1950s, when several companies developed transistors with electrodes on opposite sides of a germanium membrane that was between 4 and 100 μm thick (1, 2).

Today, single-crystal device quality membranes of semiconductors a few microns and less in thickness have found application in nearly every field of electronic technology. Such thin membranes can be used directly as substrates for making devices. These devices can be of conventional design, and rely on the extreme thinness of the membrane substrate to reduce the parasitic impedances of the devices enabling them to operate at higher frequencies than similar devices on thicker wafers (3). In circuits that have components that must operate at very different potentials, it is necessary to isolate these different potential regions. Thin single-crystal membranes coated on one side with an insulating layer (such as an oxide or nitride) can be etched to produce electrically isolated islands supported by the insulating layer. This technique is called "dielectric isolation" (4). Complementary metal oxide semiconductor (CMOS) devices made on thin single-crystal silicon substrates have also been shown to have extraordinarily high resistance to nuclear radiation (44).

Alternately, devices with novel designs that can only be made on thin membranes can be constructed. Such devices can have contacts on both the front and back surfaces of the membrane, and promise to operate at substantially higher frequencies than conventional devices on thicker wafers (5). Membranes can also be used as substrates for making devices that have specialized functions that formerly had to be performed by discrete devices. The ability to produce thin membranes in a thick wafer enables the integration of these special devices with circuits on the rest of the wafer. An example of such a device is a thermal converter for measuring rms ac signal levels. Construction of a thermal converter on a thin membrane in the wafer with the signal generation circuits eliminates the need for an external, discrete thermal converter. This results in cost savings due to the reduction of the costs of packaging the discrete device, and also leads to more efficient operation of the final circuit. Such a monolithic thermal converter is used commercially, for example in the Hewlett Packard 3336 broad band frequency synthesizer (6).

Silicon membranes have even been found indispensable in making conventional devices on thick wafers. In order to reduce parasitic impedances of devices, it is necessary to make them smaller. Currently there is a great interest in devices with dimensions less than the wavelength of light (less than 0.2 μm line widths). Since these devices are difficult to produce using conventional ultraviolet light photolithography, x-ray, electron beam, and ion beam lithography are being used. While it is possible to write the desired patterns directly on the substrate with a focused electron or ion beam, such direct writing dictates that the patterns be exposed serially, at a great cost in time. Patterns with very small geometries can be etched in very thin, large area silicon membranes. This permits the simultaneous exposure of many patterns across an entire wafer by illumination of the wafer through the mask with a large diameter, unfocused electron, or ion beam. In addition to saving time, such a system does not need expensive beam control optics. Silicon membranes can be used to make masks for x-ray lithography because they can be made very thin and uniform in thickness, they are structurally strong even when thin, and since silicon has a small atomic number, they are quite transparent to x-rays (7). Because

the range of electrons and ions in silicon is quite small, silicon membranes also have been found useful in making "see through masks" for use in electron and ion beam lithography and in making direct, photoresistless depositions of metal patterns on substrates (8).

Semiconductor membranes have also found application in making solar cells and optical detectors. The semiconductor materials used in these applications must have long carrier lifetimes so that electron-hole pairs created by photons have time to migrate to the contacts where they can be collected. Thin membranes with high crystalline quality can have recombination times close to, if not the same as, those achievable in bulk wafers. The thinness of the membrane, however, means that the distance to the contacts can be significantly less than in a thicker wafer. Thus, a higher percentage of the electron hole pairs created by the incident light will be collected at the contacts of a solar cell or detector, resulting in higher conversion efficiencies for such devices on thin membranes (9). In the case of solar cells, there is an added advantage in using thin membranes in that they require less material per unit area than comparable thick wafers. This can greatly decrease the cost per unit area for making the solar cells. This is a significant factor in large solar cell arrays that produce large amounts of power.

The surprising strength of single-crystal semiconductor membranes, even when they are only a micron or less in thickness, has enabled people to make a variety of electromechanical devices on them, including pressure sensors (10-14). Cantilevered beams made by etching away three of the edges of a membrane, leaving it attached to a thick substrate on only one edge have been used to make accelerometers (15), light modulators (16), and miniature switches (17, 18). Thin membranes can also be used as the starting material for making essentially one-dimensional freestanding wires of single-crystal semiconductors. In addition to having interesting mechanical properties, these wires have interesting electrical properties (112).

These are but a few of the many applications that have been found for micron and submicron thick single-crystal semiconductor membranes. Many more uses for them have been found and are summarized in excellent review articles by Petersen (19) and Kaminsky (20).

This article will examine the various techniques that have been developed for producing thin, freestanding, single-crystal semiconductor membranes. Only techniques for producing freestanding, single-crystal membranes of semiconductors that have thicknesses between a few nanometers and a few microns will be discussed. Such structures will be referred to as "semiconductor membranes" without repeating the qualifiers every time. Therefore, the large body of research that deals with the fabrication of amorphous or polycrystalline semiconducting films, or with the fabrication of single-crystal films of semiconductors that are intimately attached to, and fundamentally inseparable from, some substrate, such as heterostructures grown by molecular beam epitaxy (MBE) or organo-metallic chemical vapor deposition (OMCVD) techniques will not be covered.

Techniques for making single-crystal semiconductor membranes.—There are two general classes of techniques for producing semiconductor membranes that are a few microns or less in thickness. One can either start with a thick single-crystal wafer of semiconductor and etch it away to give a thin membrane, or one can grow the thin semiconductor film on a dissimilar substrate from which the semiconductor membrane can later be removed. Historically, the first class of techniques developed more rapidly, because of the lack of suitable techniques for growing thin layers of semiconductors that were of high purity and high crystalline quality. This first class of techniques will be reviewed in the next section. Recently, however, the second class of techniques has received much attention because the development of the techniques of epitaxial growth, MBE, and OMCVD has enabled people to grow extremely high quality crystalline films of semiconductors on a wide variety of substrates. The use of these epitaxy techniques to produce thin membranes of semiconductors is reviewed in the last section of this paper.

Self-limited Etching Techniques

One of the simplest techniques for producing thin semiconductor membranes is to start with a thick wafer that is 50-100 μm or greater in thickness, and dissolve it in an isotropic etching solution (21). Since many semiconductors, such as silicon and GaAs, become transparent to visible light when they become thin, one can shine light through the semiconductor during etching, and remove it from the etching solution when it reaches the appropriate thickness (22-24).

This technique unfortunately suffers from several drawbacks. It is very difficult to produce extremely uniform membranes because there is no fundamental process that stops the dissolution. Thus, for example, relative variations of a percent or less in the initial thickness of the wafer (a few microns in a wafer 100 μm or more in thickness) can lead to substantial nonuniformities of the thickness of the membranes, especially when the membranes are only a few microns or less in thickness. Such nonuniformities can also be produced if there are impurity gradients or defects in the semiconductor that cause the etching solution to dissolve different regions of the semiconductor at different rates. This can result in thin membranes that etch through in some places while being too thick in others.

Another drawback to this technique is the great difficulty in using it to produce very thin membranes, less than 1 μm in thickness. Since even the slowest etching solutions dissolve semiconductors at rates of tens of nanometers per minute, it is necessary to terminate the etching very abruptly when trying to make such thin membranes. While such control is possible with anodic etching techniques, it is nearly impossible to achieve with chemical etching solutions.

These difficulties inspired the development of "self-limited" etching techniques. The basis of these techniques is that one surface of the starting wafer is treated so that the properties of a layer of controlled thickness near that surface will not dissolve. This treated surface layer is often referred to as the "stop layer." This has the great advantage that the wafer does not have to be removed from the etching solution abruptly when the wafer becomes thin. In addition, membranes of uniform and controlled thickness will be produced even if the initial wafer is of nonuniform thickness, or if different parts of it etch at different rates. Another advantage of these techniques is that the final thickness of the membranes can be controlled and determined in advance of etching by controlling the thickness of the treated surface layer.

The most important part of these techniques is the selection of the method of treating the thin surface layer to render it insoluble in the etching solution. This treatment must not be incompatible with the end uses of the membrane; if the membranes are to be of the same electrical and crystalline quality as the initial wafer, the method of treating the surface must be reversible.

Two different processes have been developed for treating the surface of the wafer to render it insoluble in etching solutions. One process is to chemically alter the properties of a thin surface layer of the semiconductor so that it will not dissolve in the etching solution. Such chemical limiting techniques are discussed in the next two sections. The other process is to change the electrical properties of the thin surface layer so that it will not dissolve. These electrical limiting techniques are discussed in the following sections.

Chemical Limiting Techniques

Chemical limiting techniques generally rely on the fact that the dissolution rates of semiconductors in certain etching solutions are functions of the donor or acceptor impurity concentrations. Thus, one can make thin membranes of the semiconductor by creating a thin layer of the slower etching type of semiconductor on a wafer of the faster etching type, and then dissolving the bulk wafer. Two of these chemical limiting techniques have been developed for producing silicon membranes. One relies upon the fact that strongly basic amine-complexing agent solutions and alkali metal hydroxide solutions dissolve silicon

with a low impurity concentration much more quickly than silicon with a high impurity concentration; this technique is discussed in the Heavily doped stop layers section. The other technique utilizes a solution of hydrofluoric acid, nitric acid, and acetic acid that dissolves high conductivity (i.e., heavily doped) silicon, but not lower conductivity (i.e., lightly doped) silicon; this technique is discussed in the Lightly doped stop layers section. Both of these techniques surprisingly have been found to work only for silicon and not even for such chemically similar semiconductors as germanium.

Heavily doped stop layers.—In the early 1960s people discovered that solutions of highly basic amines such as hydrazine and a complexing agent, such as pyrocatechol, dissolved silicon (25). While investigating the dissolution mechanisms of silicon these amine-complexing agent etching solutions, Finne and Klein (26) found that silicon doped with more than 5% germanium would not dissolve in a solution of 3g of pyrocatechol dissolved in 17 ml of ethylene-diamine and 8 ml of water (often referred to as the EPW solution). They noted that it was possible to make membranes of silicon-germanium, by epitaxially growing a thin layer of silicon with about 5% germanium on a silicon substrate wafer, and then dissolving away the substrate.

Later, Greenwood (27) and Bohg (28) found that while this solution dissolved moderately doped n- and p-type silicon, it would not dissolve silicon doped with more than $7 \times 10^{19}/cm^3$ [0.1 atomic percent (a/o)] of boron. Greenwood was actually able to produce thin membranes of boron doped silicon (see Fig. 1). Later it was discovered that silicon highly doped with boron would not dissolve in aqueous and alcoholic solutions of KOH (29) and NaOH (30). More recently, Ipri (31) and Palik *et al.* (32) found that silicon doped with high concentrations of phosphorus also did not dissolve in either the KOH or NaOH solutions; experiments by Reisman *et al.* (33) indicate that silicon doped with high concentrations of phosphorus may not dissolve in the ethylenediamine-pyrocatechol-water solution either.

Recently, Tarng (34) has discovered a rather novel implementation of this technique. Rather than etching the silicon wafer with a chemical etching solution, he placed the wafer in a furnace maintained at a temperature of over 550°C, in an atmosphere of a gaseous refractory metal fluoride, such as tungsten fluoride. The tungsten fluoride reacts with the silicon to form a metallic tungsten layer and SiF_4, which is a gas. Tarng found that at temperatures over 550°C, this reaction will proceed until an entire wafer has been consumed and replaced with a tungsten film, provided the density of phosphorus in the substrate is less than $10^{19}/cm^3$. Silicon with a phosphorus concentration in excess of $10^{19}/cm^3$ does not react with the tungsten fluoride. Tarng was able to make thin membranes of silicon by creating a heavily phosphorus-doped layer on one surface of a moderately doped silicon wafer. This wafer was then exposed to the hot tungsten fluoride in a reaction chamber maintained at about 700°C. The bulk of the wafer reacted with the tungsten fluoride, and dissolved into gaseous SiF_4, leaving behind a film of tungsten. The reaction ceased when the tungsten film reached the heavily phosphorus doped layer. The tungsten film was then discovered in a solution of potassium ferricyanide and potassium hydroxide which did not dissolve the silicon, leaving behind a thin freestanding membrane of single-crystal silicon.

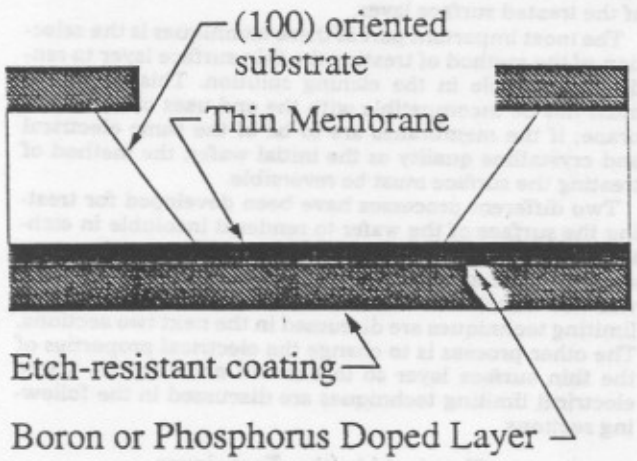

Fig. 1. Illustration of the formation of thin silicon membranes using the heavily doped stop layer technique. A high concentration of boron or phosphorus is introduced into a thin layer near the surface of a (100) oriented wafer of silicon (shown as the dark gray region above. After the deposition of an etchant-resistant layer to act as an etch mask, the silicon is etched in either a solution of ethylenediamine, pyrocatechol, and water (EPW solution) or a solution of KOH in water or alcohol. This dissolves the substrate leaving the thin heavily doped membrane. The etch mask is then dissolved in a solution that does not attack the silicon.

There is still an open discussion in the literature about why these etching solutions dissolve lightly doped silicon, and not heavily doped silicon. A very thorough series of experiments by Palik *et al.* (32), explains many aspects of the phenomenon. They propose that the smaller etch rate of heavily doped silicon in these solutions is due to the formation of an unhydrated, passivating oxide; this oxide does not form on silicon with smaller concentrations of boron or phosphorus. More recently, Raley *et al.* (35), questioned this theory, and proposed another theory based on the kinetics of the oxidation reduction reaction in the dissolution of silicon. The theory of Raley *et al.* is unfortunately based upon the results of one experiment which they did not completely report in their paper. In order to fully understand the mechanisms responsible for the success of the chemical limiting technique, more experiments remain to be done to reconcile these two theories.

Implementation.—The practical aspects of the production of thin membranes of silicon with this technique are quite straightforward. Etching solutions of hydrazine, pyrocatechol, and water; or ethylenediamine, pyrocatechol, and water; or sodium hydroxide; or potassium hydroxide all etch silicon in similar ways: they are all highly anisotropic, which means that they dissolve the (100) planes faster than the (110) planes, which in turn dissolve faster than the (111) planes. In addition, the etch rate of unhydrated SiO_2 (such as thermally grown or densified anodic oxides) in all of these solutions is very low.

To make membranes using this technique, one usually thermally oxidizes both sides of a moderately doped p-type (100) oriented silicon wafer. The resulting oxide layer serves as a mask to both define the areas into which the boron or phosphorus is to be introduced on one side of the wafer, and define the areas to be etched on the opposite side of the wafer. After oxidation, one removes the oxide from one surface of the wafer in the regions that one wishes to create the stop layer. The stop layer generally has a very high boron concentration (greater than about $7 \times 10^{19}/cm^3$) produced either by diffusion or ion implantation. In the case of the alkali metal hydroxide solutions, this layer can alternatively have a very high concentration of phosphorus. Since one needs a higher concentration of phosphorus than boron in the stop layer to obtain the limiting effect, it is often easier to create a heavily boron doped, rather than a heavily phosphorus doped, stop layer. The advantages and disadvantages of the two types of stop layers will be discussed further in the Disadvantages paragraph later in this section.

If diffusion was used to introduce the boron, a boron-silicon phase layer forms at the surface. This layer must be removed (36, 37), and then a protective oxide must be grown on the boron-diffused surface. One can alternately evaporate a layer of chromium or some other metal that does not dissolve in the etching solution (38) to protect this back surface from the etching solution. Holes are then made in the oxide on the undiffused side of the wafer, and the wafer is immersed in the etching solution. One of the simplest etching solutions that can be used is a 44 w/o potassium hydroxide in water solution maintained at about 40°C

(39). This solution contains alkali metal ions, however, which have a highly deleterious effect on MOS integrated circuits. In situations where the presence of alkali metal ions would be incompatible with the end uses of the membranes, the amine-pyrocatechol solutions, such as the one developed by Crishal and Harrington (25), Finne and Klein (26) or one of the several solutions reported by Reisman *et al.* (33), are used. These solutions are extremely sensitive to oxygen, and must be used in closed refluxing systems in an atmosphere of dry nitrogen. In addition, they have to be used at considerably higher temperatures than the potassium hydroxide solution, often at temperatures of 100°-118°C. The dissolution rate of silicon in these solutions is extremely sensitive to the concentration of impurities in the ethylenediamine, such as pyrazines, which act as catalysts for the dissolution reaction (33).

After the bulk silicon is dissolved away, thin highly boron- or phosphorus-doped silicon membranes covered with oxide are left behind. Since the covalent radius of boron is less than that of silicon, boron-doped membranes are under enormous tensile stress; the oxide however, has two oxygen atoms for every silicon atom, and tries to expand the membrane. These forces cause the membrane to buckle as shown in Fig. 2a. The oxide layer can be removed in a hydrofluoric acid solution (40). After removal of the oxide, the membranes lie perfectly flat as shown in Fig. 2b, for they are under tensile stress.

Advantages.—This technique can produce membranes with thicknesses between a few tens of nanometers, and several tens of microns. While the membranes produced using this technique have high concentrations of boron or phosphorus, they can be made very flat over very large areas, sometimes as large as an entire 2 or 3 in. wafer. As noted above, these membranes are under great tensile stress. They are as a result, very flat, and not warped. Membranes made using this technique can be used directly to fabricate x-ray masks, see-through masks for electron and ion beam lithography, or diaphragms for pressure sensors, to name just a few applications.

It should be noted that in general, regardless of the technique used to make them, square or round semiconductor membranes get extremely fragile when their average diameter exceeds about 1,000-10,000 times their thickness. Thus, it is possible to thin an entire 2 in. diam wafer to a thickness of about 10 μm, and experience relatively little difficulty in handling it. The maximum practical diameter for a 100 nm thick membrane, however, is about 1 mm. Membranes in excess of this diameter are exceedingly fragile, and apt to break along cleavage planes at the slightest mechanical shock. In general, silicon membranes are quite resilient, and with care and special handling, one can actually process (*e.g.*, perform photolithographic patterning procedures on and make electrical contacts to) silicon membranes that are less than 50 nm thick, and nearly 1 mm in diam. Membranes of other semiconductors, such as GaAs, however, tend to be very much more fragile.

Disadvantages.—The large concentrations of boron or phosphorus in the membranes severely limit the use of this technique in applications that involve active electronic devices on the thin membranes, or that require the membrane to be of high crystalline quality. Unfortunately, the concentration of boron in the silicon required to keep the silicon from etching is so high that the resultant lattice strain is greater than the maximum ($3 \times 10^{19}/cm^3$) that the silicon lattice can accommodate without the formation of dislocations, and the films consequently have a high concentration of defects (41).

Yeh and Joshi (41) reported that it was possible to reduce, if not entirely eliminate, the strain (and consequent dislocations) in the films by diffusing simultaneously with boron, an impurity such as tin which, when incorporated substitutionally into the silicon lattice would expand the lattice just as much as the boron contracted it. This technique can be made to work provided the boron concentration is small enough that the amount of tin required to compensate the strain is less than the solid solubility of tin in silicon, which is only a few times $10^{19}/cm^3$ (42). Subsequent researchers (43, 14) used this technique, known as strain compensation, to produce membranes doped with boron and germanium that had less strain than the purely boron doped membranes.

Because neither germanium nor tin are electrically active in silicon, the films still had resistivities less than approximately 1.7×10^{-3} Ω-cm, which rendered them unsuitable for most device applications. Both the strain and the resistivity of the membranes can be reduced at the same time by co-diffusing an impurity, such as antimony, with opposite electrical activity from boron, which has a larger covalent radius than boron. While this will give membranes that have higher resistivities than the uncompensated membranes, the carrier mobilities in the resulting membrane will be quite low because of the high impurity scattering, and construction of electronic devices that operate at any appreciable speed will be very difficult (45).

The high boron concentration in the membranes can be reduced without introducing compensating impurities by annealing the membranes at a high temperature for a long time to cause the boron to diffuse out of the membrane into the bulk wafer. Huang and van Duzer (46) annealed their membranes in a furnace at 990°C in a nitrogen atmosphere. They claimed that they were able to reduce the boron concentration by a factor of over 7000 to less than $10^{16}/cm^3$ using this procedure, although they presented no evidence that they had succeeded in doing so. It should be noted that the small cross-sectional area of the membranes greatly reduces the bulk diffusion velocity of impurities. Thus, to reduce the boron concentration to levels of about $10^{16}/cm^3$ could take several days even at temperatures over 1000°C (47). The diffusion time may actually be less than this, if the surface diffusion coefficient of boron in silicon is rather larger than the bulk diffusion coefficient as it is in germanium (48). This technique, therefore, may be a prac-

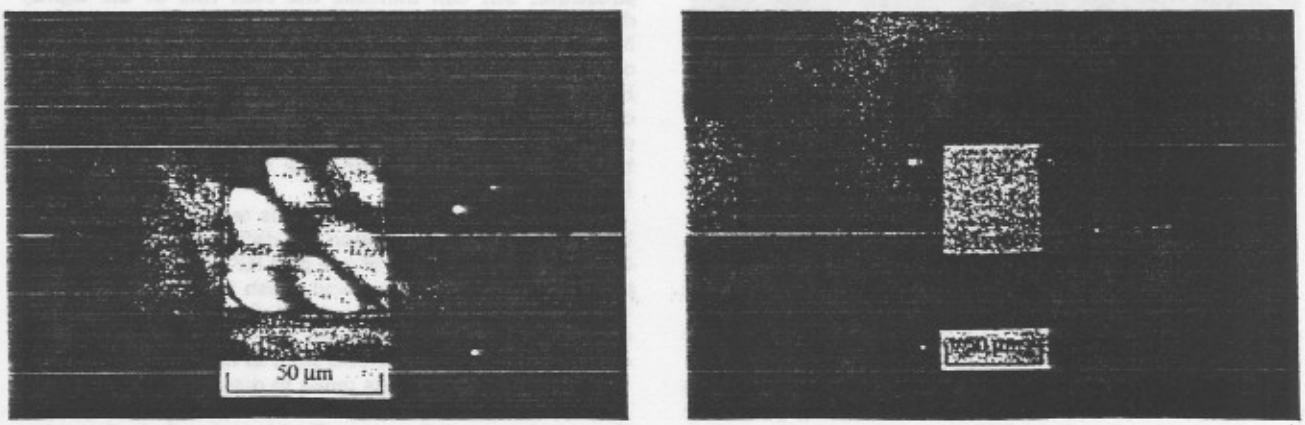

Fig. 2. Phase contrast optical micrographs of a thin boron-doped silicon membrane made by etching a silicon wafer in the EPW solution. (a, left) The phase contrast makes visible the buckling of the membrane due to the protective oxide coating on the unetched side of the membrane. The membrane is 50 μm on an edge. (b, right) After removal of the oxide, the membrane lies perfectly flat, with no observable buckling.

tical way to decrease the boron concentration in the membranes.

It should be remembered, however, that the concentration of boron necessary to stop the dissolution of the membrane is so high that dislocations necessarily form. The resulting membrane therefore has many crystallographic defects (see Fig. 3). While it may be possible to decrease the concentration of boron in the membranes by annealing them, many of these defects are thermally stable, and may take a long time to heal, even at high temperatures. It should also be noted that the healing of these defects will be slower in an unsupported membrane than in a similar layer on a thick substrate. In such a heavily doped defect-laden layer on a thick substrate, the undamaged bulk silicon wafer acts as a template upon which the damaged lattice can regrow; this, however, is not true of a thin membrane. This technique may be somewhat more effective for phosphorus doped membranes, because, unlike boron, phosphorus does evaporate from the surface.

Another drawback to extended annealing of the thin membranes to reduce the boron concentration is that when silicon membranes are heated for long periods of time at temperatures over about 1100°C, they tend to evaporate (49). The evaporation tends to leave a very pitted surface. In addition, if the membranes are heated at lower temperatures in the range of 900°-1100°C in an atmosphere from which all the oxygen or water vapor has not been removed, the water vapor will react with the silicon to form volatile silicon monoxide, also leaving a pitted surface (50, 111).

Conclusion.—The technique of utilizing heavily doped stop layers can be used to produce silicon membranes that are single crystal, and between a few tens of nanometers and several tens of microns thick. The membranes do, however, have a very high concentration of either boron or phosphorus. Because of the many difficulties involved in reducing these high impurity concentrations, this chemical limiting technique is not generally used to produce membranes for use in electronic circuits that require high carrier mobilities. It has been most widely used in applications where the electrical quality of the membranes is not of the utmost importance, such as in making large area micron thick silicon membranes for use as x-ray masks, and in making electromechanical devices such as electrostatically deformable membranes (51). It is interesting to observe that although this technique has been very widely used for making silicon membranes, no corresponding technique has been found for use with any other semiconductor, such as germanium or gallium arsenide. This is undoubtably related to the fact that very few semiconductors other than silicon form a native passivating oxide.

Lightly doped stop layers.—There is another chemical limiting technique for producing thin silicon membranes, but its mechanism is quite different from that of the previously described technique (52). Unlike the previously described technique, however, this one utilizes an etching solution that readily dissolves heavily doped silicon, but only slowly dissolves lightly doped silicon.

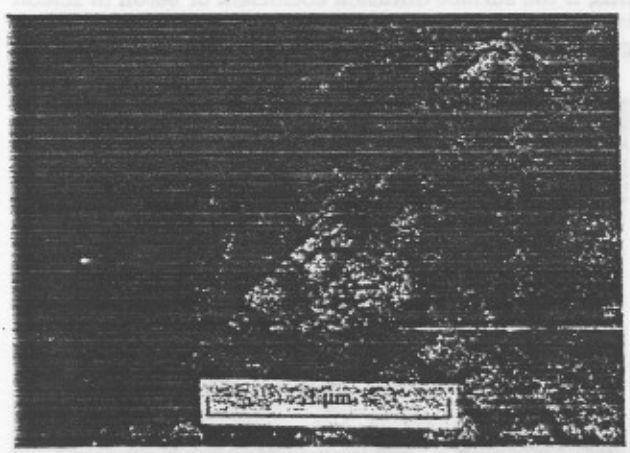

Fig. 3. Bright field transmission electron micrograph of a silicon membrane made by dissolving a silicon wafer containing a heavily boron doped surface layer in the EPW solution. The dark lines are dislocations that formed to relieve the stress created in the membranes by the very high concentration of boron.

In 1973 Muraoka and co-workers (52) investigated the dissolution rates of both n- and p-type silicon with different resistivities in a solution composed of 1 part 48% by weight hydrofluoric acid, 3 parts 70% by weight nitric acid, and 8 parts glacial acetic acid. They found that while the dissolution rate of heavily doped silicon with a resistivity of 10^{-2} Ω-cm or less was between 0.7 and 3 μm/min, that of more lightly doped silicon with a resistivity greater than about 6.8×10^{-2} Ω-cm was barely measurable. Thin membranes of silicon could thus be produced by etching heavily doped substrate wafers with lightly doped diffused or epitaxial layers on them. While Muraoka *et al.* were able to make memoranes from wafers with diffused layers, they found that lightly doped diffused layers did etch slightly; they found that epitaxial layers did not dissolve at all, giving much better limiting action, and making it easier to form thin membranes.

Advantages.—The lightly doped stop layer technique can be used to produce membranes that are greater than about 1 μm in thickness, lightly doped, and free from crystallographic defects. As a result, the membranes can be used directly as substrates for the production of active circuit elements, such as transistors and diodes. Barth (47) used membranes produced using this technique to make dielectrically isolated bipolar and MOS integrated circuits, and pressure sensors.

Another major advantage of this technique is that it is perhaps the simplest of any of the self-limited etching techniques to implement. The most demanding part of the process is the production of the necessary doping gradient, either by diffusion or, preferably, by epitaxy. Actual fabrication of the membrane is performed by etching the wafer in the solution of hydrofluoric, nitric, and acetic acids mentioned above. Unlike the ethylenediamine-pyrocatechol-water solution, this solution is not sensitive to oxygen and water vapor in the atmosphere, and therefore no special precautions need be taken to keep it under an atmosphere of dry nitrogen. The etching process can be conducted at room temperature, unlike the one using the KOH solution discussed previously. Finally, there is no need to make good ohmic contacts to the specimen in the corrosive environment of the etching solution, as is the case with electrically passivated and anodic etching techniques to be discussed in subsequent sections.

Disadvantages.—These advantages notwithstanding, the lightly doped stop layer technique does have a few limitations. One of these is the autocatalysis of the dissolution process by the dissolution reaction products. As silicon dissolves in the etching solution, the nitric acid is chemically reduced, and one of the products of the reaction is nitrous acid, HNO_2. The presence of nitrous acid does not significantly affect the dissolution rate of the highly doped substrate, but can increase the etch rate of the lightly doped epitaxial layer by as much as a factor of 40 [see Muraoka, Ref. (52), Fig. 2]. Muraoka observed that addition of an agent such as H_2O_2 or NaN_3 that decomposes the HNO_2 as it is formed will minimize this effect. This effect can also be minimized by simply using a very large volume of etching solution in comparison to the amount of silicon being etched, and agitating the solution very well [see Ref. (47), p. 20].

A more serious drawback to this technique is the similarity of this etching solution to a defect etch first reported by Dash (53) composed of one part HF to three parts HNO_3 to ten parts glacial acetic acid. Dash found that this solution tends to preferentially etch defects in a silicon wafer: crystalline silicon is dissolved rather slowly, but the silicon in the vicinity of defects such as dislocations, precipitates, and stacking faults tends to dissolve rapidly, giving rise to large etch pits. The etching solution used to make the membranes differs from Dash's etch only in that it has eight parts, rather than ten parts of glacial acetic acid. Thus, if one is to make membranes with this technique,

the thin, lightly doped layer must be absolutely free from defects: any crystallographic defects in the layer will rapidly dissolve, resulting in large irregular holes in the membrane.

Making such defect-free layers is not as easy as it might at first appear. For this limiting technique to work, the substrate has to have a very high impurity concentration. Unless special care is taken, dislocations will be present in the substrate, as discussed in the Heavily doped stop layers section in the context of the highly doped membranes produced with the EPW and KOH etching solutions. Of all the possible doping impurities, the covalent radius of arsenic in silicon is closest to that of silicon (54). Wafers with high concentrations of arsenic, very low concentrations of crystallographic defects, and relatively little strain can therefore be made. It is necessary to have low defect density in the substrate for several reasons: if the substrate etches nonuniformly, the resulting membrane will have severe thickness nonuniformities. Second, even though the epitaxial layers have very low impurity concentrations, and can theoretically be grown free of defects, any large concentration of defects in the substrate will propagate during epitaxial growth into the epitaxial layer, and a rather thick layer (as much as several microns thick) may have to be grown before the defects disappear.

Epitaxial layers grown on defect-free substrates will also have low defect densities, and can be made quite thin. While membranes produced on such wafers will be the most uniform of any produced with this technique, they still are not very uniform in thickness. Barth showed that even under the best conditions, 10-15% thickness variations in a membrane 3 μm thick were not uncommon. The membranes produced using this technique generally tend to have etch pits, or a so-called "lemon-peel finish" [see Fig. 7 and 8 of Ref. (52)].

There is also a limit to the minimum thickness of the membranes made using this technique. The substrates must necessarily be heavily doped, preferably with arsenic. When one attempts to grow lightly doped layers on such substrates, the arsenic, because of its rather high vapor pressure, tends to diffuse out of the substrate into the layer (outdiffusion) and also, the substrate dopant tends to evaporate and redeposit in the layer during growth (autodoping). The combined effects of these two processes increase the dopant density in the layer to nearly the same level as in the substrate until the layer gets to be more than about one micron in thickness [see Ref. (47), p. 78, Fig. 4.3a]. It may be possible to minimize these effects by growing the layer with low temperature molecular beam epitaxy techniques, but it is not generally possible to entirely eliminate them, especially in view of the high volatility of arsenic. It is very difficult to grow epitaxial layers that are less than 1 μm in thickness, and that have the requisite impurity concentration profile: to date, the thinnest membranes made using this technique have been a few microns or more in thickness; membranes made using this technique are commonly in the range of 3 to about 30 μm in thickness.

Conclusion.—In summary, the lightly doped stop layer technique is excellent for producing membranes that are not highly doped, are of excellent electrical quality, and greater than about 1 μm in thickness. The technique is extremely simple to implement. Membranes that are several microns or more in thickness can be readily produced. Provided that care is taken during the epitaxial growth of the lightly doped layer, thickness nonuniformities can be kept down to a few hundred nanometers, which will be negligible in membranes that are 5 or 10 μm or more in thickness. The membranes thus produced are largely free from strain, and can be used to produce electromechanical devices as well as MOS, bipolar, and dielectrically isolated integrated circuits.

Selective Etching

The techniques described in the previous sections have all involved treating a surface layer of a semiconductor wafer so that it would not dissolve in an etching solution. Another approach to the problem of producing very thin

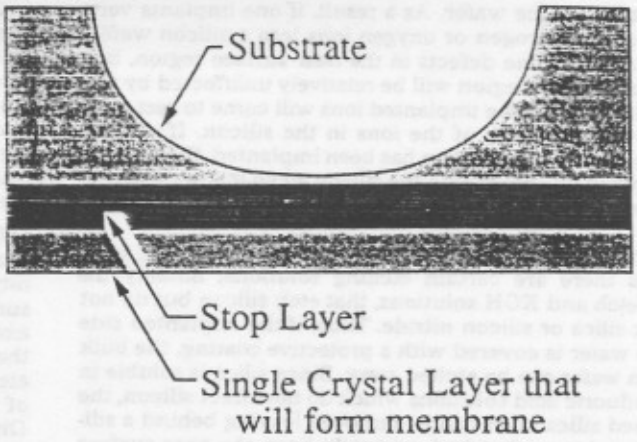

Fig. 4. Membranes formed using the selective etching techniques are generally etched in an isotropic etching solution. Before etching, a thin stop layer that does not dissolve in the same solution that dissolves the substrate is formed within the semiconductor. This stop layer can either be amorphous, such as an implanted SiO_2 layer in a silicon wafer, or it can be a single-crystal semiconductor, such as an $Al_xGa_{1-x}As$ layer on a GaAs substrate. This layer separates the substrate, which is to be dissolved away, from a single-crystal surface layer that will form the membrane. After removal of the substrate, the stop layer is selectively dissolved in an etching solution that does not attack this single-crystal surface layer, leaving it behind as a thin membrane.

single-crystal semiconductor membranes is to introduce an intermediate layer between the material that is to become the membrane and the substrate wafer (see Fig. 4). This can be done by growing epitaxially thin layers of different semiconductors with different properties on a substrate wafer, and then selectively dissolving the substrate and the unwanted intermediate layers to leave behind a thin membrane. Alternately, an impurity that reacts with the semiconductor can be implanted deep into the semiconductor to form a barrier layer. The substrate and this deep buried layer can then be dissolved in different etchants, leaving behind the desired thin membrane.

GaAs/AlGaAs stop layers.—In 1979, Griffiths and coworkers (55) observed that a solution composed of 1 part hydrogen peroxide to 19 parts ammonium hydroxide dissolved GaAs, but did not attack $Ga_{0.4}Al_{0.6}As$, and that a solution of one part HF to one part water dissolved the $Ga_{0.4}Al_{0.6}As$, but not the GaAs. Since the lattice constants of GaAs and $Ga_{0.4}Al_{0.6}As$ are very nearly the same, they used the technique of organo-metal chemical vapor deposition to produce a GaAs wafer with an epitaxial layer of $Ga_{0.4}Al_{0.6}As$ on one side, and a GaAs layer on top of that. They then dissolved the GaAs substrate in the ammonium hydroxide solution. Dissolution stopped when the $Ga_{0.4}Al_{0.6}As$ layer was exposed to the solution; the wafer was then immersed in the HF solution, and the $Ga_{0.4}Al_{0.6}As$ layer was dissolved, leaving behind the epitaxial GaAs layer as a free-standing membrane. Griffiths and his coworkers were able to produce membranes as thin as 500 nm with this technique.

The electrical quality of the membranes produced using this technique is very high, and Vokes *et al.* were able to make high frequency field effect transistors on them (56). The uniformity and thickness of the membranes produced using this technique is limited only by one's ability to grow uniform, defect-free layers of GaAs and $Ga_{1-x}Al_xAs$. This technique can, in principle, be applied to any pair of semiconductors with nearly identical crystal structures and lattice constants, for which selective etching solutions can be found. It is related to the technique often called peeled film technology, discussed later in this paper.

Implanted stop layers.—When extremely high energy ions are implanted into a semiconductor, they initially lose most of their energy to electronic excitations, rather than nuclear collisions (57). Because the ions have so much energy, very few if any come to rest in the region very near

the surface of the wafer. As a result, if one implants very high energy nitrogen or oxygen ions into a silicon wafer, there will be some defects in the near surface region, but the near surface region will be relatively unaffected by the implant. Most of the implanted ions will come to rest near the projected range of the ions in the silicon. If a sufficiently high concentration has been implanted, the oxygen or nitrogen will react with the silicon when it is annealed at high temperature, to form a buried silica or silicon nitride layer.

As mentioned in the section on chemical limiting techniques there are certain etching solutions, notably the EPW etch and KOH solutions, that etch silicon but do not attack silica or silicon nitride. Thus, if the implanted side of the wafer is covered with a protective coating, the bulk silicon wafer can be etched away. Since silica is soluble in hydrofluoric acid solutions which do not affect silicon, the exposed silica layer can be removed leaving behind a silicon membrane that had originally been the near surface region of the wafer.

Such a technique has been used by Abernathey *et al.* (58) to produce membranes of silicon that were less than 1 μm in thickness. The membranes produced using this technique are largely single crystal, but may have a small amount of residual damage in them, and may have a small concentration of oxygen or nitrogen atoms. This may be detrimental in some applications that require the highest perfection in crystalline and electrical quality of membranes.

Conclusion.—Selective etching techniques can generally be used to make membranes with a wide range of thicknesses, from less than 1 μm to several tens of microns. In addition, these techniques can be applied to a large number of different semiconductors, as the above examples illustrate. When epitaxy is used to create the stop layer, the resulting membranes are of the highest electrical and crystalline quality. When implantation is used to create the stop layer, the membranes may have some residual defects. Generally, however, the membranes need not have very high concentrations of donors or acceptors, and have fairly high crystalline and electrical quality.

Anodic Etching

The development of electrical limiting techniques received a great impetus from the discovery of the transistor in 1948. Electrical limiting techniques sprung directly from the understanding of electrical conduction processes in semiconductors developed during and after the Second World War. In 1954, Brattain and Garrett (59) discovered that holes were consumed when germanium dissolved in an anodic etching solution. Later, Turner (60) deduced the mechanism of anodic dissolution of germanium in acid (0.1*N* H_2SO_4) and alkaline (1*N* KOH) solutions to be

$$Ge + 2\ holes + 2\ OH^- \rightarrow Ge(OH)_2^{++} + 2\ electrons$$

Later work confirmed that nearly all semiconductors, including silicon, GaAs, and other III-V compounds, had very similar dissolution mechanisms in anodic etching solution, despite the fact that the actual solutions used were often quite different. Work by Turner (61, 62) and later by Memming and Schwandt (63) showed that the silicon dissolution mechanism in a dilute solution of hydrofluoric acid (<1*N*) was similar to that of germanium

$$Si + 4H_2O + 4\ holes \rightarrow Si(OH)_4 + 4H^+$$

$$Si(OH)_4 + 6HF \rightarrow H_2SiF_6 + 4H_2O$$

In 1965, Gerischer (64) showed that GaAs also dissolved in an anodic etching solution with the consumption of holes

$$GaAs + 6\ holes + 10\ OH^- \rightarrow GaO_2^- + AsO_3^{-3} + 5H_2O \text{ (alkaline solutions)}$$

$$GaAs + 6\ holes + 6X^- \rightarrow Ga^{+3}\text{ (Aq)} + AsX_6^{-3} \text{ (acid solutions, of the form HX)}$$

Although these exact dissolution mechanisms were not known until the 1960s, people were aware already in the 1950s that holes were consumed in the anodic dissolution of semiconductors. Thus, it was apparent that, by reducing the availability of holes in a thin surface layer of a semiconductor, the dissolution rate of that layer in an anodic etching solution could be drastically reduced. The bulk wafer could therefore be etched away anodically, leaving behind the thin layer as a free-standing membrane.

Junction-limited etching.—One way of reducing the availability of holes in a thin layer near the surface of an n-type semiconductor is to build a Schottky diode on one surface, and reverse bias it. The hole concentration will be exceedingly small in the depletion region formed under the Schottky barrier. When such a wafer is anodically etched, the bulk of the wafer, with a normal concentration of holes, will dissolve in an electrolytic etching solution. Dissolution will cease, however, when the depletion layer near the Schottky diode is exposed to the etching solution. This will result in the formation of a thin free-standing membrane, as shown in Fig. 5. Since the thickness of the depletion layer is a function of the reverse bias applied to the Schottky diode, the thickness of the resulting membranes can be controlled to hundredths of a micron or better by carefully adjusting the reverse bias on the diode.

Bradley (1) and Tiley and Williams (65) were perhaps the first to use this technique to make thin germanium membranes in 1954. They electroplated zinc on one side of a 5 Ω-cm n-type Ge wafer, forming a Schottky barrier. The Schottky diode was then reverse biased to create a depletion layer near the surface of the Ge that was approximately 4 μm thick. This layer was depleted of holes, so that when the Ge wafer was exposed to an electrolytic etching solution composed of 2g $NaNO_2$ (sodium nitrite) per liter, the bulk Ge dissolved, but the depletion layer did not, resulting in the formation of a thin Ge film, with a thickness approximately equal to that of the depletion layer.

This technique can also be implemented with a reverse biased p-n junction, as the hole concentration in the depletion region of the p-n junction is also very small. Use of a p-n junction to limit the dissolution, however, cannot be used to produce membranes as thin as the Schottky barrier technique, because the thickness of the resulting membrane will be equal to the thickness of the depletion layer plus the thickness of the n-type material that forms one side of the junction.

Advantages.—This junction limited etching technique is one of the only self-limited etching techniques for which

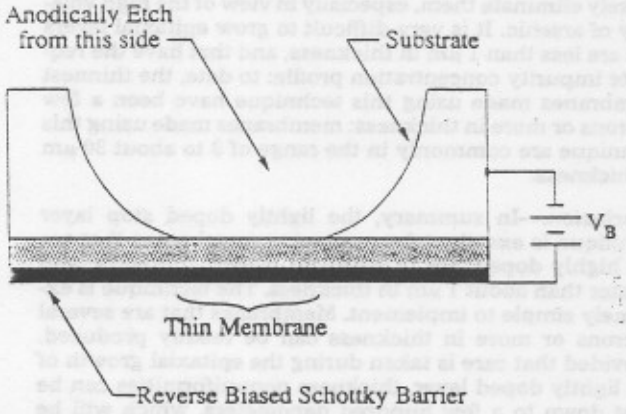

Fig. 5. The junction-limited etching technique relies upon the high electric field in a reverse biased Schottky barrier diode to reduce the hole concentration in a thin surface region of a semiconductor wafer (shown as the gray shaded region above). Since holes are consumed when a semiconductor is anodically etched, the bulk semiconductor wafer (assumed in the above drawing to be n-type) will dissolve, but the thin surface region will not, leading to the formation of a thin single-crystal semiconductor membrane with very high electrical quality. The metallic rectifying contact of the Schottky barrier (black rectangle) can be dissolved in a solution that does not attack the semiconductor after the formation of the membrane.

the final membrane thickness can be selected so simply while the etching is in progress. All other techniques require that in advance of etching, a diffused or epitaxial layer of the desired thickness be grown on a substrate that is later dissolved away. With this technique, the thickness of the membrane is selected simply by choosing the potential applied to the Schottky barrier or p-n junction and can be continuously varied. Another advantage of this technique is that the membranes are, almost by definition, of device quality: in order to make the membranes, one had to have been able to make a working electronic device, either a Schottky barrier diode, or a p-n junction on them. Since the anodic etching solution used to make these membranes is isotropic (i.e., it etches silicon at a constant etch rate independent of the orientation of the wafer), it can be used to make membranes on wafers of any conceivable orientation. Unlike the chemical limiting techniques described in previous sections, this technique is generally applicable to all semiconductors that can be doped n- or p-type, on which Schottky barriers or p-n junctions can be made, and for which suitable electrolytic etching solutions exist.

Disadvantages.—While the junction-limited etching technique is very versatile, it requires that high quality electrical contacts, both ohmic and rectifying (Schottky or p-n junctions) be made to the semiconductor in highly corrosive solutions (HF solutions in the case of silicon). This can be a difficult task that requires some experience to master; it is, however, not an impossible job. There are also limits to the thickness of the membranes that can be produced using this technique. The thickness of the depletion layer is inversely proportional to a power of the doping density and directly proportional to a power of the applied voltage (66). Thus, for a given dopant density, one can only vary the thickness of the depletion layer between its zero bias value and its value at reverse breakdown. This means that for moderate doping densities in the range of 10^{15} to $10^{16}/cm^3$, the minimum membrane thickness will be about 1 μm. The depletion layer at zero bias can be decreased to less than a few hundred nm by increasing the dopant concentration to more than $10^{18}/cm^3$. At these high impurity densities, however, one must begin to worry about the effects of lattice strain, as described earlier in the sections on chemical etching.

There is another disadvantage to this technique, which is a disadvantage inherent in all of the anodic etching techniques described in this paper, except the etch-to-voltage technique described in a following section. The limiting mechanism with these techniques is the reduction in the supply of holes to the thin layer on the back surface of the semiconductor. Thickness nonuniformities in the starting wafer or hillocks developed during etching may not disappear as etching progresses. When the depletion layer is exposed to the electrolyte, these thickness nonuniformities will give rise to hillocks on the membrane, as shown in Fig. 6. These hillocks will not dissolve, for holes are unable to flow from the electrical contact to the anodic etching power supply through the depletion layer to the hillocks. This can result in substantial thickness nonuniformities in the membranes. This problem can be solved by shaping the surface of the wafer, either by grinding or ultrasonic machining, so that the depletion layer is first exposed to the electrolyte at the bottom of the etch pit. As etching proceeds, the walls of the etch pit uniformly recede exposing more of the depletion layer. In this way, highly uniform and smooth membranes can be made.

Conclusion.—The junction-limited etching technique is the first of all the techniques described so far that can be applied to semiconductors other than silicon. It can be used to produce very smooth membranes with very few thickness nonuniformities. It is not sensitive to crystal orientation, and can be used to produce membranes with almost any orientation. While the thickness of the membranes can be varied by varying the bias applied to the Schottky barrier during etching, the final thickness of the membranes is a function of the dopant density, so that one can make moderately doped membranes several microns or more in thickness, or very thin membranes that are quite heavily doped. It is not possible directly to make membranes that are less than 1 μm thick that are not very heavily doped with this technique, although it may be possible to remove dopants in heavily doped membranes after they have been etched by annealing them, as discussed in the section on the Heavily doped stop layers.

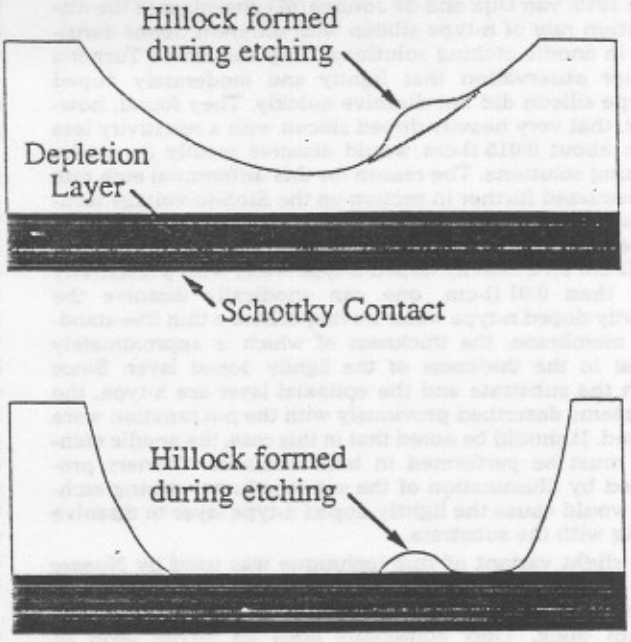

Fig. 6. Illustration of the formation of hillocks on a thin membrane made using the junction-limited etching technique. Irregularities in the etched surface (a, top) give rise to hillocks on the stop layer (b, bottom). When the stop layer (in the above illustration this is the depletion layer of the Schottky barrier) is exposed to the electrolyte, the hillocks stop dissolving, since electrical contact with the substrate has been broken: holes cannot flow through the stop layer. Hillocks can also be formed in this way on membranes made using the damage-limited etching and resistivity gradient limiting techniques. In those cases, there is no Schottky barrier, and the gray region in the above drawing represents the ion-bombardment damaged region, or the high resistivity n-type layer, respectively.

Resistivity gradient limiting technique.—Another way to reduce the concentration of holes near one surface of a semiconductor wafer is to make that layer n-type. Due to the presence of donor impurity atoms, an n-type semiconductor has an excess of electrons and the concentration of holes in an n-type semiconductor is consequently quite small. Indeed, Turner (61) found that the naturally large concentration of holes in p-type silicon enabled it to be anodically etched in a solution of 5% by weight hydrofluoric acid; because of the very low concentration of holes in n-type silicon, however, it dissolved only slowly, if at all, in the anodic etching solution. This large difference in anodic etch rates between n- and p-type silicon can be used to make free-standing n-type membranes by creating a thin n-type layer, either by diffusion or epitaxy, on a p-type substrate, and anodically dissolving the p-type substrate. This technique turns out to be rather difficult to apply directly to making n-type silicon membranes on a p-type substrate. If electrical contact is made to the p-type substrate during anodic etching, the p-n junction formed between the substrate and the thin n-type epitaxial layer will be forward biased, and holes will be injected from the p-type substrate into the n-type layer, causing it to dissolve. If the electrical contact is made to the n-type layer, the p-n junction will be reverse biased. The electrical potential available for etching is essentially the difference between the applied potential and the potential drop across the p-n junction, which will be very small. Very little current will flow, and the dissolution rate of the p-type substrate will consequently be very low. In addition, the etched surfaces will not be very smooth.

In 1970, van Dijk and de Johnge (67) investigated the dissolution rate of n-type silicon with different donor densities in anodic etching solutions. They confirmed Turner's earlier observation that lightly and moderately doped n-type silicon did not dissolve quickly. They found, however, that very heavily doped silicon with a resistivity less than about 0.015 Ω-cm would dissolve readily in anodic etching solutions. The reason for this differential etch rate is discussed further in section on the Etch-to-voltage technique. Thus, if one epitaxially grows a thin layer of lightly doped n-type material with resistivity higher than 0.3 to 0.5 Ω-cm on a heavily doped n-type wafer with a resistivity less than 0.01 Ω-cm, one can anodically dissolve the heavily doped n-type wafer leaving behind a thin free-standing membrane, the thickness of which is approximately equal to the thickness of the lightly doped layer. Since both the substrate and the epitaxial layer are n-type, the problems described previously with the p-n junction were solved. It should be noted that in this case, the anodic etching must be performed in total darkness. Carriers produced by illumination of the semiconductor during etching would cause the lightly doped n-type layer to dissolve along with the substrate.

A slight variant of this technique was used by Nuesse and Gannon (68) to make uniform, blemish-free membranes of n-type $GaAs_{1-x}P_x$, $0 \le x \le 1$ between 2 and 10 μm thick. They epitaxially grew an n-type layer of $GaAs_{1-x}P_x$ on a substrate of p-type GaAs and dissolved the p-type GaAs substrate, leaving a free-standing $GaAs_{1-x}P_x$ membrane. While one of the factors in their success was the difference in hole concentrations in the substrate and the $GaAs_{1-x}P_x$ layer, the fact that the substrate and the membrane were of different semiconductor materials was crucially important. The different electrical properties of the $GaAs_{1-x}P_x$ and the GaAs eliminated the problems with hole injection from the substrate to the membrane mentioned above. Indeed, Nuesse and Gannon experienced difficulty in making n-type GaAs membranes from n-type GaAs layers on p-type GaAs substrates. In this case, the n-type GaAs membrane tended to dissolve, albeit at a slower rate than the p-type GaAs substrate.

There are several reasons why they had more success making $GaAs_{1-x}P_x$ membranes than GaAs membranes. The bandgap of $GaAs_{1-x}P_x$ is appreciably larger than that of GaAs. Thus, the intrinsic electron concentration in $GaAs_{1-x}P_x$ will be significantly less than that in GaAs. Consequently the injected hole current from the GaAs into the $GaAs_{1-x}P_x$ will be much smaller than from p-type GaAs into n-type GaAs. Since the anodic etch rate is proportional to the hole current, the smaller injected hole current in the $GaAs_{1-x}P_x$ layers will cause the dissolution to stop more effectively at the $GaAs_{1-x}P_x$ layers than at the GaAs layers. In addition, the hole diffusion coefficient in $GaAs_{1-x}P_x$ is less than that in GaAs, which will further reduce the ability of holes generated in the $GaAs_{1-x}P_x$ from migrating to the electrolyte-semiconductor interface. Thus, while Nuesse and Gannon's technique does rely on the difference in majority carrier types in the substrate and the membrane, it was also necessary for the substrate and membrane to be of different materials with different electrical properties. Because of this, Nuesse and Gannon's technique can also be considered to be related to the technique of selective etching described in the section on Selective etching.

Advantages.—While van Dijk and de Johnge and other subsequent researchers have applied this resistivity gradient limiting technique to making membranes of silicon, it is applicable to any semiconductor that can be doped n- or p-type, and for which the hole concentration in lightly doped n-type material is small enough that it will not dissolve appreciably in an anodic etching solution. The membranes made using this technique can commonly be made as thin as 1 μm and can have excellent electrical and structural quality. While the membranes made using this technique are n-type, they have such a low donor concentration that one can easily change the conductivity without sacrificing carrier mobilities by introducing suitable electrically active impurities. One can even make the membranes p-type by implanting or diffusing a p-type impurity (69). The membranes made using this technique have been used fairly widely for making MOS transistors (70, 71), arrays of p-n junctions for vidicon targets and dielectrically isolated integrated circuits (4), dE/dx detectors (72), as well as for particle channeling studies (73).

Disadvantages.—While it is a fairly simple matter to use the resistivity gradient limiting technique to make membranes that are on the order of several microns to several tens of microns in thickness, it is very difficult to make membranes 1 μm or less in thickness. Meek *et al.* (73) made membranes that were 0.7 μm in thickness by first making a membrane from a wafer with a 1-2 μm thick epitaxial layer. The membrane was then either etched in a solution that etches silicon very slowly, or was carefully oxidized, and the oxide subsequently dissolved in hydrofluoric acid. It is very difficult, if not impossible, to produce a thin membrane less than 1 μm in thickness directly using this technique. In order to do so, it would be necessary to produce a very lightly doped epitaxial layer that was less than 1 μm in thickness on a very heavily doped wafer. The difficulties with doing this were described in the discussion of the Lightly doped stop layers chemical limiting technique (47).

One way of avoiding having to grow epitaxially such a thin lightly doped layer on a heavily doped substrate is to introduce a compensating (p-type) impurity into a thin layer of the heavily doped n-type substrate either by diffusion or implantation. While it is possible to achieve a sufficiently large difference in conductivity between the substrate and the diffused layer so that membrane formation is possible, extreme care must be taken to introduce the correct concentration of impurity: too large a concentration would make the back surface p-type, and it would dissolve even faster than the heavily doped substrate; too small a concentration of the compensating p-type impurity would not increase the resistivity of the n-type substrate enough to cause limiting. In any event, the large compensating concentrations of n- and p-type impurities in the membrane would make the carrier mobilities quite small, making the membrane unsuitable for use in making high-speed electronic devices.

One problem particular to Nuesse and Gannon's technique is that the lattice constant of $GaAs_{1-x}P_x$ is different from that of GaAs, so that it is difficult to grow good quality thin single-crystal layers on GaAs without substantial densities of misfit dislocations and other defects (74, 75).

Conclusion.—The resistivity gradient limiting technique can be used to produce lightly doped n-type membranes with very high electrical and structural quality that are between one and several tens of microns or more in thickness from wafers with any crystallographic orientation. Membranes can be made of any semiconductor, including silicon, GaAs, and GaP for which the etch rate of lightly doped n-type material is significantly lower than that of heavily doped n-type material. The technique is very simple to apply, requiring only one good electrical contact to be made to the semiconductor. The most crucial and difficult aspect of the technique is the construction of the starting wafer with a thin, high quality, defect free, lightly doped layer on a heavily doped substrate.

Damage limited etching.—One of the problems that prevented van Dijk and de Johnge's technique from being used to produce membranes of silicon less than 1 μm thick was that outdiffusion and autodoping phenomena prevented the growth of suitably thin, lightly doped epitaxial layers on heavily doped substrates. Attempts to bypass these problems by starting with a heavily n-type doped wafer and implanting a p-type impurity into it to create a thin, compensated, surface region that was effectively, lightly doped led, in 1982, to the discovery of another self-limited anodic etching technique (76). The authors attempted to etch an implanted silicon wafer that had not been annealed, and found that the dissolution rate of the implanted layer was markedly less than that of the unimplanted material (see Fig. 7).

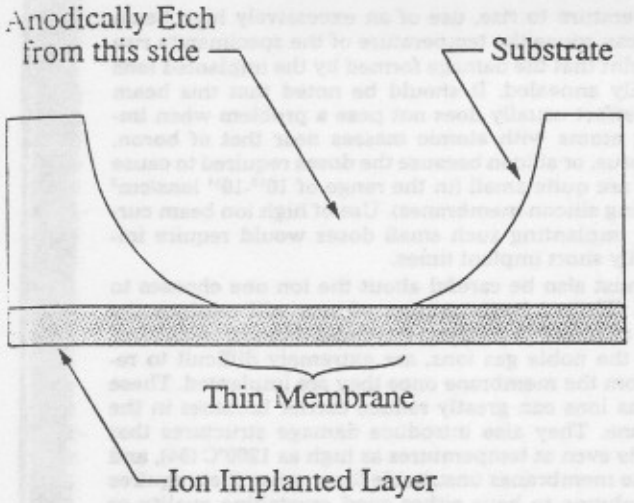

Fig. 7. The formation of membranes using the resistivity gradient or the damage-limited etching techniques is illustrated. The former technique requires that a thin, lightly doped n-type stop layer (gray region) be formed on a heavily doped n-type substrate. With the latter technique, a damaged, ion implanted stop layer (gray region) must be formed in a substrate wafer that can have any type, resistivity, or orientation. The substrate wafer is then anodically etched; since the stop layer does not dissolve in the etching solution, it is left behind as a thin membrane.

Experiments have shown that it is possible to obtain a significant difference in etch rates between implanted and unimplanted semiconductors with only a very modest implant dose. For example, it was found that silicon membranes could be produced from either n- or p-type wafers of any resistivity and orientation implanted with doses of as little as $3 \times 10^{13}/cm^2$ of 100 keV phosphorus ions. GaAs membranes could be made from wafers implanted with doses of as little as $10^{12}/cm^2$ of 100 keV neon ions (77). Membranes can be made from wafers implanted with either donor or acceptor ions, or ions that are entirely neutral in the semiconductor, such as silicon ions into a silicon wafer. Moreover, the final thickness of the membrane is related to the projected range of the implanted ions: in silicon, preliminary measurements (76) indicated that the membrane thickness was approximately equal to the projected range, while in GaAs, it was approximately twice the projected range of the implanted ion (77).

There had been sporadic observations of this differential dissolution rate between implanted and unimplanted semiconductors in the past (78, 79) but the mechanism of the effect was not well understood. It has been proposed that this limiting phenomenon is due to a reduction in the supply of holes in the thin implanted region due to the presence of carrier traps created by implantation damage (80). When high energy ions with atomic masses approximately equal to or greater than the semconductor atomic mass are implanted into the semiconductor lattice, they eventually lose enough energy through electronic interactions that they begin to collide with atoms in the lattice, displacing them from their lattice sites (81). The resultant lattice vacancies and interstitials give rise to numerous dangling bonds, which give rise in turn to a spectrum of deep levels within the semiconductor bandgap.

In many semiconductors, including silicon and gallium arsenide, these deep levels very effectively trap holes and electrons, making the resistivity of the implanted layer so high that it can be considered to be semi-insulating. The concentration of holes in this layer is consequently very small. Thus, when a semiconductor wafer with a thin implanted layer is anodically etched from the unimplanted side, the bulk material, which is unimplanted, dissolves readily in the anodic etching solution, because holes can readily flow from the contact to the electrolyte semiconductor interface. When the implanted layer is exposed to the electrolyte, however, the presence of the traps impedes the flow of holes, and the dissolution of the implanted

Fig. 8. Optical micrograph of 320 nm thick (100) oriented GaAs membrane made using the damage-limited etching technique taken with transmitted light. The membrane was made from a 0.0023 Ω-cm silicon-doped GaAs wafer implanted with a dose of $10^{11}/cm^2$ neon ions at 100 keV.

layer proceeds at an unmeasurably small rate. This results in the creation of a thin membrane, such as that shown in Fig. 8.

This thin membrane of course contains the implanted layer, and is semi-insulating. The important feature of this technique, however, is that the damaged layer can be created by implanting ions at a low enough dose that the long range crystalline order of the membrane is not destroyed. It is not necessary, and indeed not desirable, to implant such high doses that the membranes are completely amorphous. When the membranes are annealed at a high enough temperature, there is enough undamaged single-crystal material in the membranes that the somewhat isolated regions of damage can regrow using these single-crystal regions as lattice templates. In this way one can produce membranes of semiconductors that are appreciably less than 1 μm in thickness, are uniform (see Fig. 9), and free from crystallographic defects. By proper choice of the implanted ion, the membranes can have the same electrical characteristics as the original semiconductor from which they were made.

It is interesting to note that if this limiting phenomenon is due to the creation of deep traps by the implantation

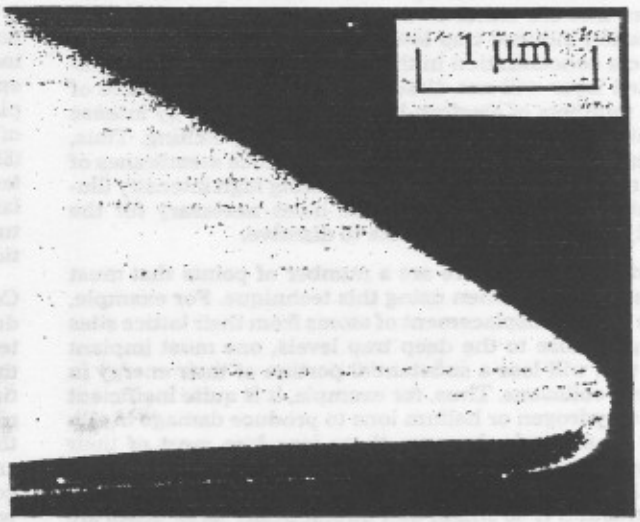

Fig. 9. Scanning electron microscope image of a cleaved silicon membrane made using the damage-limited etching technique from a 1-2 Ω-cm p-type silicon wafer implanted with $4 \times 10^{14}/cm^2$ neon ions at 100 keV. The membrane is approximately 280 nm thick.

damage, it should also be possible to produce membranes by creating deep traps by the introduction of chemical impurities. Metals such as lithium tend to reduce the hole concentration in silicon, and transition metal impurities, such as gold or titanium, are well known to create deep levels within the bandgap of silicon, effectively trapping carriers (especially holes) at room temperature (66, 82). Diffusion of a thin layer of gold in silicon would raise the resistivity of the layer to very high values. This should give a significant differential etch rate between the substrate undoped with gold and the thin gold doped layer permitting the formation of large area membranes. To the knowledge of this author, however, this experiment has not yet been done.

One problem with using transition metal atoms to create the trap levels is that, especially in silicon, these transition metal atoms tend to diffuse by an interstitial diffusion mechanism. As a result, they have very high diffusion coefficients even at moderately low temperatures, and it may be difficult to produce sufficiently thin layers to yield membranes less than 1 μm in thickness. A more serious problem with using transition metal impurity atoms to produce thin membranes is that, unless one actually wants to produce a membrane of a semiconductor doped with that impurity, it is essentially impossible to remove the impurity once the membrane is formed. In special cases, however, most notably in the case of lithium in silicon, it may be possible to remove the impurity by electromigration of the metal ions in a strong electric field. This, however, may not always be totally effective for all metals.

Advantages.—This damage limited etching technique, when ion implantation is used to create the deep trap levels, is perhaps the only technique available for directly producing self-limited membranes that are appreciably less than one micron in thickness. Since the final thickness of the membranes is related to the range of the implanted ions, implantation of very low energy ions into the semiconductor will create a very thin damaged region, which will result in the formation of very thin membranes: it has been possible to produce membranes as thin as 10-30 nm with this technique (83). In many ways, this technique is complementary to van Dijk and de Johnge's technique: while the latter can be used to produce membranes that are greater than about 1 μm in thickness, the present technique can readily be used to produce membranes that are less than about 1 μm in thickness. The maximum thickness achievable with the damage limited etching technique is determined by the maximum implantation energy that is available, and can be as much as several microns.

Like other anodic etching techniques, this technique can be used to make membranes of any crystallographic orientation. Unlike other techniques based on anodic etching, however, this technique can be used to produce membranes that are either n- or p-type. Surprisingly, the implantation induced trap levels are so effective in reducing the hole concentration in the implanted layer, that the implanted layer will not dissolve even with the presence of large numbers of electron-hole pairs generated by intense illumination of the semiconductor during etching. Thus, one can even use this technique to produce membranes of high resistivity n-type material by using high intensity illumination to optically inject the holes necessary for the lightly doped n-type substrate to dissolve.

Disadvantages.—There are a number of points that must be kept in mind when using this technique. For example, since it is the displacement of atoms from their lattice sites that gives rise to the deep trap levels, one must implant ions that will lose a substantial portion of their energy in nuclear collisions. Thus, for example, it is quite inefficient to use hydrogen or helium ions to produce damage in silicon, for example, because these ions lose most of their energy through electronic excitations. While they do lose a small fraction of their energy through nuclear collisions, this fraction is so small, that impractically large doses are necessary to achieve the requisite densities of vacancies and interstitials. One must also be careful not to use too high a beam current when implanting the ions. Since the energy deposited in the specimen by the ion beam causes its temperature to rise, use of an excessively high beam current can cause the temperature of the specimen to rise to the point that the damage formed by the implanted ions is actually annealed. It should be noted that this beam heating effect usually does not pose a problem when implanting atoms with atomic masses near that of boron, phosphorus, or silicon because the doses required to cause limiting are quite small (in the range of 10^{13}-10^{14} ions/cm^2 for making silicon membranes). Use of high ion beam currents in implanting such small doses would require impractically short implant times.

One must also be careful about the ion one chooses to implant. While a large number of ions will produce the damage required to produce good membranes, some ions, notably the noble gas ions, are extremely difficult to remove from the membrane once they are implanted. These noble gas ions can greatly reduce carrier lifetimes in the membrane. They also introduce damage structures that are stable even at temperatures as high as 1200°C (84), and make the membranes unsuitable for any use that requires the membrane to have either good crystalline quality or good electrical quality (85).

When annealing the membrane, one must remember that many semiconductors either decompose or evaporate at elevated temperatures. Silicon tends to evaporate at temperatures over 1100°C (49), and membranes cannot be annealed at such high temperatures for long periods of time without developing severely pitted surfaces, or entirely evaporating. It has been found that annealing the membranes in an RF induction furnace in high vacuum at 1000°C for periods of between 5 and 15 min is sufficient to heal the damage in phosphorus implanted silicon membranes (3). GaAs tends to decompose with evolution of As even at such low temperatures as 500°-600°C. As a result, one must take special precautions to prevent this, such as capping the GaAs with a layer of silicon nitride (86) or annealing the membrane in an equilibrium atmosphere of arsenic (87).

One intriguing aspect of many of the self-limiting techniques based on anodic etching is that the limiting mechanism is not specific to one particular solution. For GaAs, for example, this technique will yield self-limited membranes when etched in solutions of perchloric acid and acetic acid (88), as well as in solutions of sodium hydroxide (68). One must however be careful not to choose an etching solution that preferentially etches defects in GaAs. It is the presence of deep trap levels created by the ion implantation damage that reduces the hole concentration to the point that the anodic etching rate decreases. If, however, the anodic etching solution or the etching conditions chosen, are such that defects are etched preferentially, the resulting membrane can have very many etch pits, and may perhaps dissolve completely.

This damage limited etching technique can be used to produce membranes of many different semiconductors, including silicon and gallium arsenide. It cannot be simply applied to all semiconductors, however. For instance, implantation damage in germanium results in the formation of a trap level that is only 0.05 eV above the valence band (89). This makes the implanted layer highly p-type at room temperature. This, when combined with the naturally large hole concentration in germanium at room temperature (due to its small bandgap) results in the rapid dissolution of the implanted layer at room temperature.

Conclusion.—The use of ion implantation damage to produce thin semiconductor membranes is perhaps the only technique besides the heavily doped stop layer technique that can directly produce membranes that are substantially less than 1 μm. The damage limited etching technique, however, is the only self-limited etching technique that can produce membranes that are this thin and have crystalline and electronic quality approaching the level common in commercially available bulk semiconductor wafers. In addition, damage limited etching is one of the only techniques that can produce membranes from either n- or p-type, high resistivity, or even intrinsic material in the thickness range 10-1000 nm. Like other self-limiting techniques based on anodic etching, it is not orientation

dependent, and is applicable to a wide variety of semiconductors.

Etch-to-voltage technique.—The anodic etching techniques discussed so far relied upon the reduction in the hole concentration in a thin layer near one surface of a semiconductor wafer to reduce the dissolution rate of that layer in an anodic etching solution. Another way of producing a thin membrane from a thick semiconductor wafer would be to start with a high resistivity n-type wafer that does not etch readily in an anodic etching solution, and treat the bulk of the wafer so that it dissolves. The untreated portion of the wafer then remains behind as the thin membrane. This essentially is the principle behind the etch-to-voltage technique.

As discussed earlier, holes are consumed when silicon is dissolved in an anodic etching solution. Normally, n-type semiconductors have an excess of electrons, and therefore have a very low concentration of holes. As a result, n-type semiconductors do not dissolve very quickly in anodic etching solutions. The etching solution, however, is conducting, although with somewhat low conductivity. The result is that a Schottky barrier is formed at the interface between the semiconductor and the etching solution, as shown in Fig. 10a. In an anodic etching solution, the n-type semiconductor is connected to the positive terminal of a power supply. Thus, the Schottky barrier formed at the interface between the semiconductor and the electrolyte is reverse biased. This tends to reduce the supply of holes at the surface of the semiconductor, and hence its etch rate, even more.

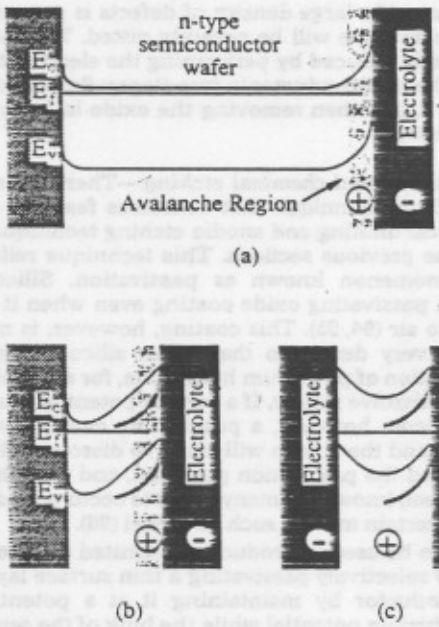

Fig. 10. Illustration of the formation of semiconductor membranes using the etch to voltage technique. (a) A high voltage is applied to the semiconductor so that avalanche breakdown occurs in the depletion region (gray dotted area) of the reverse biased Schottky barrier formed at the interface between the electrolyte and the n-type semiconductor wafer. The carriers generated in this avalanche region cause the semiconductor to dissolve. In these figures, E_c represents the conduction band energy, E_f the Fermi energy, and E_v the valence band energy. (b) When the wafer becomes so thin that the avalanche region gets close to the opposite side of the wafer (protected from the electrolyte by an insulating coating), the electric field (related to the slope of the energy bands) decreases below the value necessary to sustain avalanche breakdown (indicated by the dotted line). In the absence of avalanche breakdown, there are no carriers available for etching, and dissolution of the semiconductor stops, resulting in the formation of a thin membrane. (c) When both sides of the wafer are etched, the potential distributions and electric fields are symmetrical about the center of the wafer. In the limit of small membrane thickness, the potential distributions will be nearly uniform, and the electric fields will be very small inside the membrane; in the absence of carriers generated by avalanche breakdown, the membrane will not dissolve.

If a large enough reverse bias is applied to the semiconductor, however, the electric field in the depletion region near the semiconductor-electrolyte interface will get large enough that avalanche breakdown will occur. This breakdown will produce very large concentrations of electrons and holes, and the semiconductor will be able to dissolve. The voltage at which breakdown occurs is a function of the donor density in the semiconductor: the higher the donor density, the smaller the breakdown voltage (66). For a donor density of about $10^{18}/cm^3$ in GaAs, the breakdown voltage is about 4V; for a donor density of $10^{16}/cm^3$ (also in GaAs), it increases to about 70V. Both of these values are for GaAs in a solution of H_2O:H_3PO_4 with $2.6 < pH < 3.0$ (90).

It should be noted that this is the fundamental reason for the limiting observed with van Dijk and de Johnge's resistivity gradient limiting technique discussed above. The breakdown voltage for the heavily doped n-type substrates used by van Dijk and de Johnge was less than the applied etching potential. Holes generated by the resulting avalanche breakdown in the substrate enabled it to dissolve. The breakdown voltage for the lightly doped epitaxial layer, on the other hand, was much higher than the applied potential. Thus, when the heavily doped substrate was dissolved away exposing the lightly doped epitaxial layer to the etching solution, dissolution would cease because the applied potential was not high enough to cause avalanche breakdown in the lightly doped epitaxial layer, and there were not enough holes in that layer otherwise to cause it to dissolve.

Now consider the anodic dissolution of a homogeneous wafer of n-type semiconductor as shown in Fig. 10a. First consider the case in which only one side of the wafer is exposed to the electrolyte. Assume that a potential is applied to the semiconductor that is just above the minimum voltage that would cause avalanche breakdown in the bulk wafer. The charge carriers generated in this avalanche region, shown as the light gray dotted region at the right of the figure, will enable the wafer to dissolve.

In this figure, the opposite surface of the semiconductor is assumed to be protected from the electrolyte by an insulating coating. The presence of surface states at this surface will cause the Fermi level to be fixed near the middle of the bandgap. When the bulk of the wafer has dissolved, and the back of the breakdown region begins to get close to this surface of the wafer, as shown in Fig. 10b, the energy of the bottom of the conduction band will approach the value determined by the density of surface states, rather than the lower value in the bulk semiconductor determined by the density of donors. The slope of the conduction band will therefore decrease. Since the electric field is related to the slope of the conduction band, the electric field will also decrease. The electric field will actually decrease below the value necessary to sustain the avalanche breakdown, as shown in Fig. 10b, and dissolution of the semiconductor will cease, resulting in the formation of a thin membrane. The thickness of the membrane will be on the same order of magnitude as the width of the avalanche breakdown region in the bulk semiconductor.

If both sides of the semiconductor wafer are exposed to the electrolyte (Fig. 10c), the potential distribution will be symmetrical about the middle of the wafer. As the wafer gets thin enough that the breakdown regions from opposite sides of the wafer touch, the electric field will decrease below the value necessary to sustain breakdown, and etching will cease. In this case, the thickness of the membrane will be on the order of twice the width of the breakdown region in the bulk semiconductor. It should be noted that in the limit of small membrane thickness, the potential across the membrane will be uniform, there will be little if any electric field in the membrane, and the membrane will not dissolve in the anodic etching solution.

Advantages.—The etch-to-voltage technique is unique amongst all those described in this paper in that it produces membranes with what one might call uniform electrical thickness. In other words, the electrical breakdown voltage at every point of the membrane will be the same.

Thus, if there are variations in the donor density in the membrane, there will be corresponding variations in the actual thickness of the membrane so that the electrical breakdown voltage will be constant throughout the membrane. This property makes this technique exceedingly useful for making thin membranes for constructing electronic devices. In fact, its earliest use was in thinning n-type GaAs layers grown epitaxially on semi-insulating GaAs substrates to create layers with uniform breakdown voltage. Such thinned layers were found to be superior for producing very high frequency modified Read IMPATT diode structures (90).

The thickness of the layers or membranes produced using this technique can of course be varied by varying the donor density in the membranes: the higher the donor density, the less the minimum voltage required to produce breakdown, and the thinner will be the resulting membranes. A more versatile way to control the thickness, however, is with the applied bias. While there is a lower limit to the voltage that must be applied to the semiconductor before it will etch, one can apply voltages higher than this. The higher the applied voltage the thinner the resulting membrane. This can be understood with reference to Fig. 10b. For a given applied bias, the semiconductor will get thinned to a thickness where the electric field is less than that required for breakdown to occur. Increasing the applied bias at this point would increase the electric field, breakdown would again occur, and etching would resume until the thickness had decreased again to the point where the electric field was less than that required to sustain the avalanche process.

One great advantage of this technique is its simplicity. While it does require one good ohmic electrical contact to be made to the semiconductor wafer, no further processing, such as the growth of epitaxial layers, formation of Schottky diodes, or the creation of damaged regions by implantation, etc., is necessary. Another great advantage of this technique is that it is applicable to a wide variety of semiconductors, from silicon to GaAs. This technique, in fact, should work for any n-type semiconductor for which the room temperature hole concentration is small enough that anodic dissolution will not occur when the applied bias is less than the breakdown voltage. If the semiconductor is being etched from only one side, the breakdown voltage must increase as the thickness of the wafer decreases. In other words, the surface states must create a p-type depletion layer at the surface, rather than an n-type accumulation layer (90, 91).

Disadvantages.—One of the major advantages of the etch-to-voltage technique can actually be a disadvantage in certain circumstances. It was noted above that this technique produces membranes that have a uniform breakdown voltage, not necessarily a uniform thickness. Thus, if there are variations in the donor density in the semiconductor, the areas of the membrane with higher donor density will be thinner than those with lower donor density. While this is advantageous for some applications, it will not be advantageous in applications that require very uniform membrane thickness.

Since the breakdown voltage is substantially reduced in the vicinity of defects in the crystal, anodic etching tends to proceed most rapidly in the vicinity of defects. This can often result in a severely pitted surface; in extreme circumstances, the membrane can actually etch through in places. Rode *et al.* (92) showed that this severe pitting could be minimized by performing the anodic etching in two stages. An anodic oxide is first grown on the wafers in a solution that does not dissolve the oxide (see reaction mechanisms for anodic etching above). The wafer is then removed, and the oxide layer is dissolved in an etching solution that dissolves only the oxide, and does not affect the semiconductor. This process is repeated until a limited membrane is obtained.

At each anodization/etching step approximately 0.1-0.2 μm of semiconductor is removed. Because of the potentially large number of anodization/etching steps required to thin a thick wafer, the wafer is usually thinned by grinding or chemical polishing to a few tenths to several hundredths of a millimeter thickness before this technique is appplied. The spatial thickness uniformity of the membranes thus produced is essentially limited by the uniformity of the donor density in the wafer. The membranes are relatively free from severe pitting. By proper choice of the reagent used to dissolve the anodic oxide, the final membrane surfaces can be made extremely clean (93).

One final note that must be emphasized is that the anodic process, whether it be anodic etching or anodic oxidation, must in the case of this technique, be performed in the dark. The presence of light illuminating the sample, whether it be due to deliberate illumination, or simply to the room lights, will give rise to optically generated electron hole pairs. If the intensity of illumination is large enough, these optically generated charge carriers will cause the semiconductor to dissolve, even though the applied potential may be less than the breakdown potential for the thin membrane, and consequently the membrane should have stopped etching.

Conclusion.—The etch-to-voltage technique is the only technique available for producing membranes with uniform electrical breakdown voltage at all points of the membrane. One consequence of this is that if there are variations in the donor density in the semiconductor, the resulting membrane will not have uniform thickness. This technique can be used to produce membranes that are as thin as a few tenths of a micron in thickness. While this technique only works on n-type semiconductors, it is applicable to a wide variety of semiconductors, including GaAs and silicon. The technique is not sensitive to the orientation of the semiconductor, but it is sensitive to the density of defects. If a large density of defects is present, the resulting membrane will be severely pitted. This pitting can be greatly reduced by performing the electrolytic dissolution of the semiconductor in two stages: first anodically oxidizing it, and then removing the oxide in a separate etching solution.

Electrically passivated chemical etching.—There is one self-limited etching technique that combines features of both the chemical limiting and anodic etching techniques described in the previous sections. This technique relies upon the phenomenon known as passivation. Silicon readily forms a passivating oxide coating even when it is only exposed to air (94, 95). This coating, however, is not continuous, or very dense, so that when silicon is immersed in a solution of potassium hydroxide, for example, the silicon will dissolve slowly. If a certain potential is applied to the silicon, however, a passivating coating will suddenly form, and the silicon will cease to dissolve. This potential is called the passivation potential, and this phenomenon has been known for many years to occur with silicon as well as certain metals, such as nickel (96).

This effect can be used to produce self-limited semiconductor films by selectively passivating a thin surface layer of the semiconductor by maintaining it at a potential above the passivation potential while the bulk of the semiconductor wafer is at a potential below the passivation potential. This can be done by creating a thin n-type layer on a p-type substrate. Ohmic contact is made to the n-type layer, and a potential equal to or very slightly greater than the passivation potential is applied between it and a cathode. The wafer is immersed in a solution that etches silicon, such as the potassium hydoxide or the EPW solution mentioned in the sections on Chemical limiting techniques. Since the passivation potential applied to the n-type layer is positive relative to the cathode, the p-n junction is reverse biased. Most of the applied potential appears across the p-n junction, and thus the potential of the p-type substrate relative to the cathode is less than the passivation potential. The p-type substrate therefore dissolves normally. When the substrate is dissolved exposing the n-type layer to the etching solution, however, dissolution ceases because the applied potential is no longer dropped across the p-n junction, and the potential of the n-type layer relative to the cathode is equal to the passivation potential. The p-type substrate therefore dissolves away leaving behind the n-type layer (97).

Advantages.—This passivation technique was first used by Waggener (97) to produce thin membranes by dissolving p-type wafers with n-type diffused layers in a KOH solution. Jackson and Wise (98) and Gealer (99) were also able to produce thin membranes from p-type wafers with n-type epitaxial layers using the EPW etching solution described in the Heavily doped stop layer section. While this technique uses the same etching solutions used with the chemical limiting techniques discussed previously, it has the great advantage that the membranes produced using this passivation technique can be quite lightly doped, and consequently have excellent crystalline and electrical quality. Most workers have used epitaxially grown n-type layers on p-type substrates to obtain membranes. As a result, most reported work with this technique deals with membranes greater than about 1 μm in thickness. It should, however, also be possible to produce membranes from diffused or implanted n-type layers on p-type substrates. Such layers could be appreciably thinner than 1 μm, and one could presumably therefore produce membranes much less than 1 μm in thickness.

This technique can also be used to make heavily doped p-type membranes from epitaxial or diffused layers on lightly doped p-type substrates, although this is much more difficult than making n-type membranes as described above. Gealer (99) and Palik *et al.* (100) measured the passivation potentials of silicon of different types and resistivities in the EPW solution and in KOH solutions, respectively. They found that the absolute values of the passivation potentials of n-type material tended to be higher by about 0.2V than p-type material, and also that the passivation potentials of heavily doped p-type material were slightly higher (≈1.2V) than those of more lightly doped p-type material (≈1.0V). One can therefore start with a wafer of fairly lightly doped p-type silicon (with acceptor density of $2 \times 10^{15}/cm^3$, for instance), and make a layer of more heavily doped silicon (with acceptor density of $4.3 \times 10^{19}/cm^3$, for example) on one surface. Application of a potential to the heavily doped layer equal to its passivation potential will cause the lightly doped p-type substrate to dissolve, leaving the heavily doped layer behind as a thin membrane.

Disadvantages.—The electrochemical passivation technique has only been demonstrated to work with anisotropic etching solutions. This means that it will work only for particular orientations of silicon, namely, (100) oriented, and perhaps also (110) oriented silicon. It should also be noted that this technique has only been demonstrated to work for silicon, and for no other semiconductor. This is presumably because silicon is the only semiconductor that forms a tough passivating oxide. While the possibility of producing lightly doped n-type membranes and heavily doped p-type membranes using this technique has been demonstrated, it does not appear possible to make lightly doped p-type membranes directly with this technique (99). It is, of course, possible to make an n-type membrane and subsequently introduce acceptor impurities into it to make it p-type.

Like the membranes produced with the lightly doped stop layer chemical limiting technique, the membranes made using this technique appear to have lemon peel-like nonuniformities in thickness. These are shown nicely in Fig. 5 of Palik's paper (100). Unlike the self-limited etching techniques based on anodic etching, hillocks formed during etching will not result in nonuniformities in the thickness of the membrane as discussed in the section on the Junction limited etching technique. It has however, been observed that the membranes produced using this technique tend to be thicker at the center than at the edges. This trench effect is described by Palik *et al.* (100). The etching conditions, however, can be controlled to reduce the magnitudes of these effects so that the uniformity in the thickness of the membranes is about 1% on a 10 μm thick membrane (thickness nonuniformities of 0.1 μm) (101).

The practical implementation of this technique requires great care. It is a rather challenging task to protect the good electrical contacts to the layer to be passivated from the highly corrosive etching solutions used in this technique. The problem is made more difficult by the fact that the solutions are used at elevated temperatures. One must also be careful that the potential distribution in the thin layer that is being passivated is uniform. If there are nonuniformities in potential, some parts of the membrane may be at a potential above the passivation potential, while others will be at a potential below it. These areas will dissolve, and the membrane will disintegrate.

Conclusion.—The electrically passivated chemical etching technique utilizes the highly anisotropic etching solutions used in the chemical limiting techniques. The membranes produced using this technique, however, are generally n-type, and have impurity concentrations orders of magnitude less than the membranes produced with the chemical limiting techniques. The electrical and crystallographic quality of the membranes made using this technique is excellent. One should be able to make membranes that are anywhere from tens to hundreds of nm to tens of microns in thickness with this technique, though to date, this technique has only been applied to making membranes greater than 1 μm in thickness. The membranes can be made uniform to better than 1% (for a 10 μm thick membrane). Because the etching solutions used to make the membranes are so highly anisotropic, the membranes are at the bottom of pyramidal etch pits, and have edges that are precisely aligned with crystallographic directions in the crystal, a fact which may be of advantage in some applications. The implementation of this technique requires good electrical contact to be made to the semiconductor in the highly corrosive environment of a high temperature (60°-120°C) etching solution, a fairly difficult task. This technique can only be used to produce silicon membranes of certain orientations [specifically, (100) and perhaps also (110) orientations], and to date, has not been extended to any other semiconductor.

Direct Deposition Techniques

The techniques described in the previous sections produced thin single crystal semiconductor membranes by dissolving thick, high quality semiconductor crystals. For many years, this was the only way of producing very thin membranes of semiconductors that were of both high crystalline quality and high electronic quality. These techniques, however, were all quite inefficient: one had to start with a thick single-crystal wafer and dissolve most of it away to produce the desired thin membrane. It would be much more efficient in the use of material, if one could grow the thin membrane directly on some substrate from which it could easily be removed later. With the advent in the 1970s of the techniques of liquid phase, vapor phase, and molecular beam epitaxy, and organo-metallic chemical vapor deposition (OMCVD), direct growth of high purity, high crystalline quality semiconductor films on a variety of substrates became possible.

Ribbon growth.—In 1980, Stirling (102) developed a process for making thin single-crystal ribbons of silicon and germanium. Amorphous silicon or germanium was continuously deposited on a PTFE or Mylar belt using low temperature RF decomposition of silane or germane. At the beginning of the belt, there was a single-crystal seed. After deposition, the belt was burned away, and the initially amorphous semiconductor ribbon was heated to the crystallization temperature by a focused infrared heater or laser beam. The ribbon grew into a long single-crystal using the seed crystal as a lattice template. Stirling used this technique to produce thin very long sheets of silicon and germanium.

While the resulting thin sheets were largely single crystal, they tended to have a high concentration of edge dislocations (103). McFarlane and co-workers (103), however, found that if one grew a thin layer of silicon or germanium epitaxially upon the silicon or germanium ribbon with chemical vapor deposition, the epitaxial layer had orders of magnitude fewer defects than the original ribbon, because the edge dislocations in the ribbon did not grow into the epitaxial layer. Inclined dislocations in the ribbon did propagate into the epitaxial layer, however, but the den-

sity of inclined dislocations was vastly less than that of edge dislocations. The epitaxial layer was of sufficiently high quality that solar cells could be made on it (104).

While the membranes made using this technique appear to be of sufficient quality to produce solar cells, the dislocations present in the ribbons and epitaxial layers grown on them preclude their use as substrates for making devices that must operate at high speed. The membranes made using this technique are generally in the range of several tens to several hundreds of microns in thickness. At the present time, it is not clear what the ultimate minimum thickness of such films can be. While this technique offers promise of producing thin membranes of single-crystal semiconductors with a minimum wastage of material, much research remains to be done to perfect the crystalline quality of the ribbons, and reduce their thickness before they can be widely used to produce high speed, high performance devices.

Dissolvable intermediate layers.—While the previously described technique is by far the most attractive economically, the membranes made in this way are generally not of suitable crystalline quality to be used for electronic devices. To get around this shortcoming and to produce thin semiconductor membranes that are large single crystals with good crystalline quality, a thin layer of the semiconductor that is to become the single-crystal membrane can be deposited epitaxially upon a thicker substrate wafer of single crystal semiconductor. After deposition of this thin layer, however, one must remove it from the substrate in such a manner that the substrate is not destroyed in the process.

One way of doing this is to grow an intermediate layer between the single-crystal substrate and the thin film that is to become the membrane. This intermediate layer should be soluble in a solvent that does not attack either the substrate or the membrane. Deutscher and Grunbaum (105), applied this technique to making silicon membranes by growing a thin silicon layer on a variety of different intermediate layers, including sodium fluoride, sodium chloride, and silver which were in turn deposited on a silicon wafer. The alkali halide intermediate layers were very thin, and were grown at an elevated temperature, so that they grew epitaxially on the silicon substrate.

Since the alkali halides used as intermediate layers were water soluble, free-standing silicon membranes could be produced by dissolving the alkali halide intermediate layers in water after deposition of the silicon layer. Deutscher and Grunbaum were able to produce membranes of silicon and silicon-germanium that were between 2 and 20 μm in thickness. The great advantage of this technique is that it is very economical of silicon: one only uses enough silicon to create the membrane, and the substrate is reusable. In addition, this technique is applicable to a number of semiconductors other than silicon.

While they do not present any evidence, Deutscher and Grunbaum claim that the membranes produced using this technique are single crystal. One disadvantage of this technique is that the sodium in the intermediate layer does readily diffuse into the silicon, even at low temperatures. This precludes using the membranes to make MOS devices. It should, however, be possible to keep the sodium concentration in the silicon sufficiently low that the membranes could be used for solar cells (105) and other devices, and as substrates for transmission electron microscopy studies.

"Peeled film" technology.—Another very similar way of separating a thin epitaxial single-crystal layer from a substrate was developed by Milnes and Feucht (9). They grew an intermediate layer of a semiconductor that had a very close lattice match to the substrate, and also had a lower melting point than the substrate on a single-crystal substrate wafer. They then grew epitaxially a layer of the semiconductor which was to become the membrane on top of the intermediate layer. When the wafer was heated, the intermediate layer melted, and they were able to peel off the top single-crystal semiconductor membrane as shown in Fig. 11. Alternately, if the intermediate layer was soluble in a solvent that did not attack either the substrate or the top

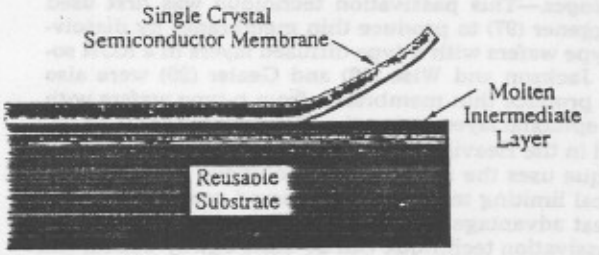

Fig. 11. In the embodiment of the peeled film technique shown in this figure, a thin layer of lower melting point semiconductor (such as GeSi) is grown epitaxially on a single-crystal wafer of another semiconductor (such as Si). A layer of silicon is then grown epitaxially on top of the GeSi intermediate layer. When the wafer is heated, the GeSi layer melts, and the top layer of silicon can be peeled off as a thin, single-crystal membrane.

semiconductor membrane, the membrane could be detached from the substrate by placing the wafer in the solvent for the intermediate layer (106).

Milnes and Feucht were able to make membranes of silicon between 1 and 50 μm in thickness by growing an intermediate layer of Ge or Si_xGe_{1-x} on a silicon wafer, and growing a 1-50 μm silicon layer on top of this. Since the Ge or Si_xGe_{1-x} melts at a lower temperature than the Si, they were able to peel off the silicon membrane by heating the wafer to a temperature of around 1000°C, at which the intermediate layer melted. The membranes thus produced were of good crystalline quality because thin layers of Si_xGe_{1-x} grow epitaxially on silicon. In addition, the membranes were of excellent electrical quality (107). Since the silicon substrate wafer was not affected by the process of producing the membrane, it was possible to reuse it to produce more membranes.

Advantages.—The peeled film technique has many advantages. It is applicable to a wide variety of different semiconductors: indeed, the only restriction is that one must be able to find a suitable combination of semiconductors that grow epitaxially on each other, and which have a suitable difference in melting points or difference in solubility in some solvent. Milnes and Feucht were able to use this technique to make membranes of silicon, CdTe, CdSe, AlSb, InP, and GaAs. Because the membranes were grown epitaxially on substrates with essentially the same lattice constant as the membrane material, they are all of the highest crystalline quality.

This peeled film technique is perhaps one of the most efficient techniques for producing good quality single-crystal semiconductor membranes that has been developed to date. There is almost no wastage of expensive single-crystal semiconductor material that must be dissolved to produce the membrane. The substrate wafer is not consumed in the process, and can apparently be reused a large number of times.

Disadvantages.—The peeled film technique does, however, have its limitations. The lower limit to the thickness of membranes that can be made this way is determined by the thickness of the intermediate layer and is about 1 μm. The final semiconductor membrane must be significantly thicker than the intermediate layer (at least a factor of 30 thicker). If it is not, the top semiconductor layer may dissolve in the intermediate layer, or, if it does not dissolve, when the membrane is peeled off, a significant amount of the intermediate layer may adhere to the membrane. The resulting structure would then be more of a composite between the top semiconductor layer, and the intermediate layer. There is also a lower limit to the thickness of the intermediate layer: if it is made too thin, it may not exhibit the melting properties that are necessary to separate the membrane from the substrate: rather, when the wafer is heated, the constituents of the intermediate layer could diffuse into the substrate and into the membrane.

After the membrane is separated from the substrate, a small amount of the intermediate layer always adheres to the surface of the membrane. If the membrane is quite thick (over 10 μm, say), this does not severely affect the

properties of the membrane. In fact, Milnes and Feucht observed that the adherence of the intermediate layer to the membrane can be used to advantage by doping the intermediate layer heavily with either acceptor or donor impurities to make the intermediate layer n- or p-type. The thin layer of the intermediate semiconductor that adheres to the membrane can then be used as an ohmic contact to devices on the membrane.

When the wafer is heated to separate the membrane from the substrate, there is some diffusion of the intermediate layer into the membrane. As noted before, this can be negligible if the thickness of the membrane is much greater than that of the intermediate layer. Cook (108) attempted to minimize the effects of diffusion in thinner films by heating the wafer to a lower temperature than the melting temperature of intermediate layer, thus minimizing the effects of diffusion. A focused laser beam was then scanned across the surface of the wafer. The laser briefly heated a localized area above the melting temperature of the intermediate layer and enabled the membrane to be separated from the substrate. Because the intermediate layer was only briefly in a molten state, the effects of diffusion were minimized.

Peeled film technique with noncrystalline intermediate layers.—While the laser melting technique of Cook reduced the diffusion of the intermediate layer into the membrane and the substrate, some of the intermediate semiconductor layer always adheres to the membrane. Bozler and co-workers (109) refined the peeled film technique to eliminate the necessity for a molten intermediate layer during the separation of the membrane from the substrate. Like Milnes and Feucht, they started with a single-crystal semiconductor substrate wafer. Upon this they deposited a growth mask. In one embodiment of their invention, they made a pattern of stripes on a photoresist layer on a GaAs wafer. They then heated the photoresist in air to carbonize it. Single-crystal GaAs was then epitaxially grown over the carbonized photoresist layer, using the exposed single-crystal substrate as a template for the lattice. After growth, the top layer and substrate were each bonded to glass plates, and the plates were separated. The thin GaAs layer broke away from the substrate, because it did not adhere to the carbonized photoresist (see Fig. 12). In their patent, Bozler *et al.* describe applications of this technique to other semiconductors and give many other implementations of this technique.

Bozler's refinement of the peeled film technology has many advantages. The constraints of having to find semiconductors with similar lattice constants that can be grown epitaxially on one another and which have suitably different melting temperatures are removed. It can therefore be applied to a large number of semiconductors. The membranes do not have to be heated to be removed from the substrate, thus minimizing diffusion of impurities. As is the case with Milnes' technique, the substrates can be reused many times without degrading.

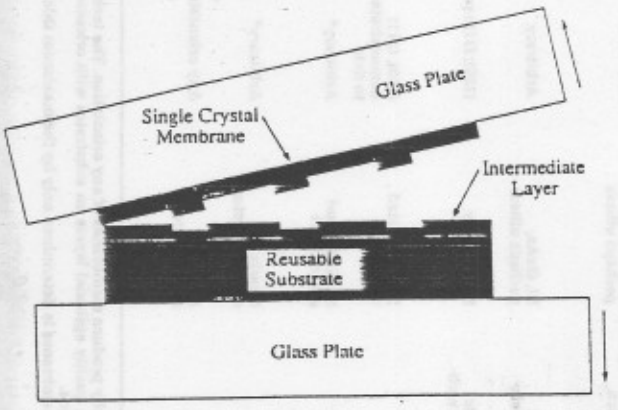

Fig. 12. Illustration of another embodiment of the peeled film technique. An intermediate layer is formed by depositing an organic compound, such as carbonized photoresist (shown as the dark gray regions), on the surface of a single-crystal semiconductor wafer. Holes are opened in this layer, and a thin layer of single-crystal semiconductor is grown epitaxially on top of the organic intermediate layer using the regions of the substrate visible through the holes in the intermediate layer as a lattice template. To separate the semiconductor membrane from the substrate, glass plates are attached (for example, with wax) to both sides of the wafer. The two plates are pried apart, and the thin membrane separates from the substrate wafer as shown.

These advantages unfortunately have a price. The membranes were attached to the substrate by pillars that extended through the windows in the carbonized photoresist layer. As a result, when the membranes are separated from the substrate, these pillars leave protrusions in the membrane, resulting in nonuniformities in thickness of the membranes. Another problem is that there is a limit to the minimum thickness of the membranes. When the membrane is grown, growth begins at the regions of the substrate that are visible through the windows in the photoresist. Growth proceeds up over the carbonized photoresist layer. The membrane does not become continuous until the thickness of the membrane is about 1 μm. Thus, this technique cannot be used to make membranes less than a few microns in thickness; indeed, membranes made using this technique are usually several tens of microns thick.

Stressed films.—A rather novel approach to peeling thin films of single-crystal semiconductors off substrate wafers was developed by Tanielian, *et al.* (110). When metals are evaporated or sputtered onto semiconductors, enormous stress is produced at the interface between the metal and the semiconductor. For this reason, metal contact layers on integrated circuits are often quite thin (<100 nm). Tanielian *et al.* found that if they deposited a nickel-chromium layer 6 or 7 μm in thickness on a very clean silicon wafer, the stress at the metal semiconductor interface would be large enough to actually peel off a thin surface layer from the silicon wafer. If the metal films were thinner than 6 or 7 μm, they did not spontaneously peel off. Layers of silicon could still be peeled off even with these thinner metal films by thermally shocking the wafer, by dropping it into liquid nitrogen, for example. After the metal film has peeled the thin semiconductor layer from the substrate, the metal can be removed in an etching solution that does not attack the silicon, leaving behind a freestanding silicon membrane.

The membranes made with this technique are single crystal and are generally 15-20 μm thick. In addition, they have low defect density. While to date this technique has only been applied to silicon, it should be possible to apply it to other semiconductors. In addition, the substrate wafer can be reused: after one surface layer has been peeled off, metal can be deposited again, and another surface layer can be peeled off. This process can apparently be repeated until the wafer is consumed. One of the greatest advantages of this technique is its simplicity: to produce membranes, one only has to deposit a very thick coating of metal on the wafer, and the semiconductor layer will spontaneously peel off!

Unfortunately, this advantage is somewhat offset by the inconvenience of having to wait for a long time while the metal is being deposited. At deposition rates typically achieved in RF sputtering and even thermal evaporation machines, one must deposit the metal for as long as 8-10h before the film thickness is great enough to peel off the semiconductor membrane. It can be fairly difficult to maintain constant deposition conditions for such extraordinarily long times. Another disadvantage of this technique is that when the metal peels off the semiconductor membrane, the semiconductor peels off along cleavage planes, which are the (110) planes in silicon. Unless the surface of the silicon wafer is oriented in the (110) direction, these cleavage planes will not be parallel to the surface. The surface of the membrane will therefore be quite jagged, with nonuniformities of as much as 2 μm in a 15 or 20 μm thick membrane (thickness nonuniformity of about 10%).

Conclusion

The number of techniques for producing thin freestanding single-crystal semiconductor membranes is nearly as

Table I. Comparison of the different techniques for producing thin single-crystal semiconductor membranes discussed in this paper

Technique	Etching solution	Membrane materials	Crystal orientation	Membrane thickness	Advantages	Disadvantages	Applications	Crystal quality	Electrical quality
Heavily doped stop layers	Anisotropic chemical etch	Si only	(100), (110) possible	10 nm-20 μm	Very large (as great as 3 in. diam) membranes; membranes very uniform in thickness	Very high impurity concentration; crystal defects common	Electromechanical devices; x ray, ion, and evaporation masks; materials science studies	Poor	Poor
Lightly doped stop layers	Isotropic chemical etch	Si only	Arbitrary[a]	<1 μm[b]	Membranes free from defects; technique simple to implement	Severe thickness nonuniformities (10-15% of membrane thickness)	Electronic devices, pressure sensors, and other electromechanical devices	Excellent	Excellent
GaAs/AlGaAs stop layers	Isotropic chemical etch	GaAs; extendable to other III-Vs	Arbitrary[a]	≤100 nm to several μm[b]	Can remove substrates leaving membranes with complex heterojunctions	Requires high quality epitaxial material; requires several etching steps	Electronic and optical devices; electron microscopy and materials science studies	Excellent	Excellent
Implanted stop layers	Isotropic or anisotropic chemical etch	Si; may be extendable to other materials	Any orientation with isotropic etch solution	Few 100 nm-few μm	Useful in dielectric isolation	Residual damage in membrane sometimes hard to remove	Dielectric isolation of circuits; materials science studies; electrochemical devices	Fair to good	Fair to good
Dissolvable intermediate layers	—	Si, Ge, III-Vs	Arbitrary	2-20 μm	Simplicity	High sodium content in membranes, impurities hard to control	Solar cells, electron microscopy, materials science studies	Poor-fair	Poor-fair
Junction limited etching	Isotropic anodic etch	Si, Ge, III-Vs	Any orientation	≤100 nm to ≥10 μm	Can vary thickness by varying bias	Electrical contact to junction is difficult	Electronic devices, electromechanical devices	Excellent	Excellent
Resistivity gradient limited etching	Isotropic anodic etch	Si, Ge, III-V compound semiconductors	Arbitrary[a]	≤1 μm-≥50 μm[b]	Very high purity membranes; can be applied to many semiconductors	Difficult to make very thin membranes	Electronic and optical devices, vidicon targets, nuclear particle detectors, dielectric isolation	Excellent	Excellent
Damage limited etching	Isotropic anodic etch	Si, GaAs, III-Vs perhaps others	Arbitrary	≤10 nm-~1 μm	Produces thinnest membranes; will work even with intrinsic material	Damage produced by some ions (e.g., noble gases) difficult to remove	Electronic, optical, and electromechanical devices; materials science studies, electron microscopy	Excellent	Excellent
Etch to voltage	Isotropic anodic etch	Si, GaAs, perhaps others	Arbitrary	<100 nm-≥1 μm	Only technique that produces constant electrical thickness	Membranes often not of uniform thickness	Electronic and optical devices	Excellent	Excellent
Electrical passivation	Anistropic chemical etch	Silicon only	(100); (110) possible	≤1->50 μm[b]	Produces very flat, very large area membranes	Electrical connections to passivated layer difficult to make in corrosive etches	Electronic, optical, and electromechanical devices	Excellent	Excellent
Ribbon growth	—	Demonstrated with Si, Ge	(100), (111) demonstrated to date	~50-200 μm	Very efficient use of material	Many defects; thick membranes	Solar cells	Poor	Poor
Peeled film technology: molten interlayer	—	Si, GaAs, and other III-Vs	Arbitrary[a]	2 to ≥50 μm[b]	Very efficient use of material; substrate reusable	Membranes have thin layer of intermediate material on one side	Solar cells	Good	Good
Peeled film technology: solid interlayer	—	Nearly all semiconductors	Arbitrary[a]	2 to ≥50 μm[b]	Very efficient use of material; substrate reusable	Membranes not of uniform thickness	Solar cells	Fair to good	Good
Stressed films	—	Any semiconductor	Any orientation	15-20 μm	Simplicity; very efficient use of material	10-20% nonuniformities in thickness; cannot control thickness; long metal deposition times	Solar cells	Good to excellent	Excellent

[a] This technique can theoretically produce membranes of any orientation. The technique, however, requires the growth of an epitaxial layer on a single-crystal substrate. Because of the difficulty of growing high quality epitaxial layers on substrates with orientations other than (100) or (111), this technique has to date only been demonstrated to produce membranes with these orientations.

[b] The upper thickness of the membranes is determined only by the maximum thickness of epitaxial layer that can be grown.

great as the number of applications for such membranes. In this review, I have described a number of techniques for producing thin semiconductor membranes (see Table I). These techniques fall into two broad classes. The first one relies upon the alteration of either the chemical or electrical properties of a thin surface layer of a bulk wafer of single-crystal semiconductor to reduce the rate of dissolution of that thin layer in some etching solution. The wafer is then etched: the bulk of the wafer is dissolved away leaving behind a thin membrane. For many years, techniques based on this principle were the only ones available for producing high quality semiconductor membranes. These techniques, however, are quite inefficient in the use of semiconductor material, for one has to grow large boules of semiconductors, cut them up into wafers, and then dissolve most of the wafer to produce the thin membrane.

With the development in the 1970s of various epitaxy techniques for growing thin films of semiconductors of high quality, a second class of thin membrane fabrication techniques became possible. Thin single-crystal layers of semiconductors could be grown on substrates with different chemical or physical properties. Thin, single-crystal intermediate layers could be grown between the substrate and the desired semiconductor membrane. These layers could be either melted, or etched away to separate the epitaxial film from the substrate, thus giving a thin, freestanding, single-crystal membrane. These techniques are generally much more efficient in the use of semiconductor material, as one grows the semiconductor membrane that one needs, and does not have to dissolve away large quantities of expensive, single-crystal semiconductor wafers. This fact makes these techniques very attractive economically, especially for such applications as solar cells, for which very large areas of good quality single crystals are necessary.

As techniques for producing thin semiconductor membranes have been developed and improved, more uses for them have been found. Today, they have found use in such diverse applications as solar cells, high frequency diodes, and electromechanical devices. As the designs of these devices improve, the requirements for thickness, crystalline quality, and purity of the membranes will grow more stringent, and without doubt, many new techniques will be developed for producing them.

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