

Characteristic-Impedance Measurement Error on Lossy Substrates

Dylan F. Williams

National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80303

Ph: [+1] (303)497-3138 Fax: [+1] (303)497-3122 E-mail: dylan@boulder.nist.gov

Uwe Arz and Hartmut Grabinski

Universität Hannover, D-30167 Hannover, Germany

Ph: [+49] 511.762.5030 E-mail: uarz, hgra@lfi.uni-hannover.de

Abstract- This paper examines error caused by parasitic inductance in the characteristic impedance measured by the calibration comparison method on lossy silicon substrates.

INTRODUCTION

We examine error in the characteristic impedance Z_0 measured by the new algorithm of [1] caused by parasitic inductance in the contact pads. We call the method the calibration-comparison method for measuring characteristic impedance, because it is based on the calibration-comparison method introduced in [2]. It is particularly well suited for measuring the characteristic impedance of planar transmission lines printed on silicon and other lossy substrates.

The most accurate method of which we are aware for measuring the characteristic impedance of planar transmission lines [3] assumes that the substrate is a lossless dielectric, and is not applicable to lossy silicon substrates. Eo and Eisenstadt [4] introduced what has become the most common way of measuring the characteristic impedance of planar transmission lines fabricated on lossy substrates. It determines Z_0 by comparing the transmission line's scattering parameters measured by a probe-tip calibration to those of an ideal transmission line.

The calibration-comparison method for measuring characteristic impedance is unique because it is

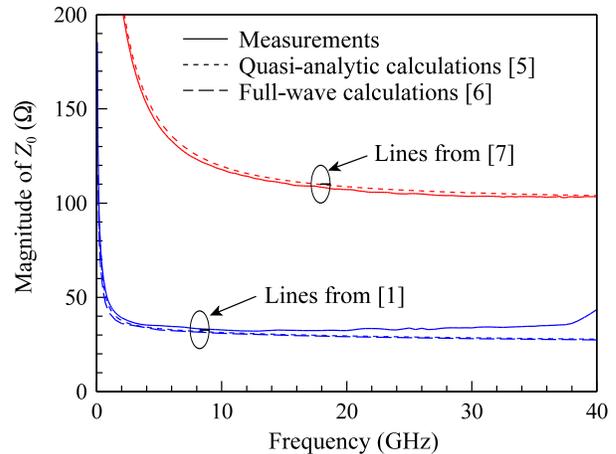


Fig. 1. Comparisons of the calibration-comparison method for measuring characteristic impedance to calculation.

insensitive to even large shunt contact-pad capacitance and conductance. Reference [1] shows that the calibration-comparison method for measuring characteristic impedance is more accurate than the method of [4]. Figure 1 illustrates the potential accuracy of the calibration-comparison method for measuring characteristic impedance. It compares measurements of the silicon transmission lines of [1] to quasi-analytic calculations using the method of [5], which solves separately for the series impedance and shunt admittance per unit length of quasi-TEM transmission lines, and to full-wave calculations performed with the method of [6]. Figure 1 also compares measurements of the characteristic impedance of the microstrip access lines fabricated in a CMOS technology and discussed in [7] to calculations performed with the method of [5]. These

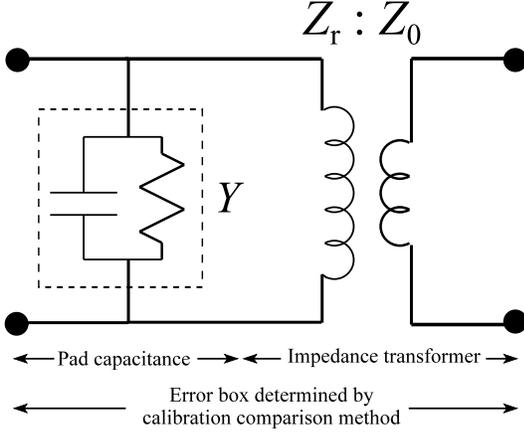


Fig. 2. The equivalent-circuit model for the contact pads and impedance transformer used in the calibration-comparison method for measuring characteristic impedance.

microstrip lines had a single 1 μm wide signal conductor on the second level of metallization centered between ground rails.

However, the calibration-comparison method for measuring characteristic impedance is based on the assumption that there is no parasitic inductance in the transition between the probe and transmission line under test. Here, we examine the effect of parasitic inductance on the accuracy of the calibration-comparison method for measuring characteristic impedance.

THE CALIBRATION-COMPARISON METHOD FOR MEASURING CHARACTERISTIC IMPEDANCE

The calibration-comparison method for measuring characteristic impedance compares a planar transmission line under test to a set of easily characterized reference lines fabricated on a low-loss substrate. The procedure begins with a multiline TRL probe-tip reference calibration [8] in the easily characterized reference lines. The reference impedance of this calibration is set to 50 Ω , and its reference plane is moved back to a position close to the probe tips using the methods described in [3].

A second-tier multiline TRL calibration in the transmission line of interest then determines a set of “error boxes” relating the second-tier calibration to the probe-tip reference calibration. These error boxes describe not only any contact-pad parasitics not accounted for by the probe-tip reference calibration, but also an impedance transformer that translates the 50 Ω reference impedance of the probe-tip calibration to the reference impedance of the second-tier TRL calibration, which is equal to the characteristic impedance Z_0 of the transmission lines we wish to characterize [9].

Figure 2 shows the simple model for the transition between a probe tip and the transmission line characterized by the method. The model consists of a lossy shunt contact pad with admittance $Y = G + j\omega C$ followed by an impedance transformer that maps the reference impedance Z_r of the probe-tip calibration into the reference impedance Z_0 of the second-tier TRL calibration. The cascade matrix X of the circuit in Fig. 2 is¹ [9]

$$X = \frac{1}{\sqrt{1-\Gamma^2}} \left(\begin{bmatrix} 1 & \Gamma \\ \Gamma & 1 \end{bmatrix} + (1+\Gamma) \frac{YZ_r}{2} \begin{bmatrix} -1 & -1 \\ 1 & 1 \end{bmatrix} \right), \quad (1)$$

where we have set all the reference impedances real and

$$\Gamma \equiv \frac{Z_0 - Z_r}{Z_0 + Z_r}. \quad (2)$$

When transition parasitics are dominated by contact-pad capacitance and conductance, the error box X' measured by the calibration-comparison method will be approximately equal to X .

The calibration-comparison method for measuring characteristic impedance implemented in [1] is based on the fact that the term multiplied by $YZ_r/2$ in (1) adds to X_{21} , but subtracts from X_{12} , so its effect cancels completely from the mean $\frac{1}{2}(X_{12} + X_{21})$. Thus, even for very large contact-pad admittances Y , $\Gamma/\sqrt{1-\Gamma^2} \approx \frac{1}{2}(X'_{12} + X'_{21})$. As a result, the estimate¹

¹These equations are printed incorrectly in some versions of [1], but are printed correctly here.

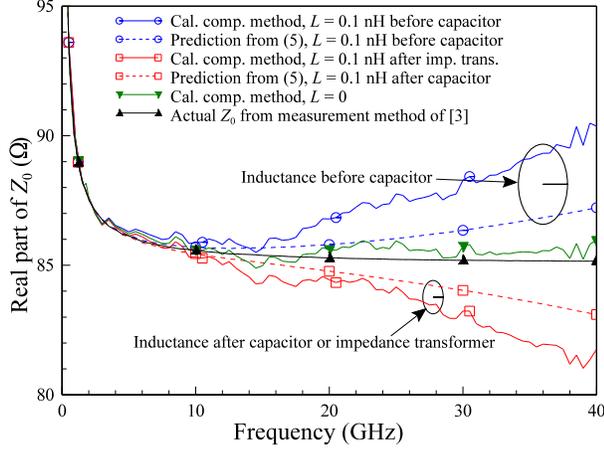


Fig. 3. Actual measurement errors compared to prediction from (5).

$$\hat{\Gamma} \equiv \sqrt{\frac{(X_{12}' + X_{21}')^2}{4 + (X_{12}' + X_{21}')^2}} \quad (3)$$

is insensitive to contact-pad admittance Y , and can be used to accurately determine Z_0 even when the contact-pad admittance is large.

INDUCTANCE ERROR

While the calibration-comparison method for measuring characteristic impedance is insensitive to contact pad capacitance and conductance, the method does not account for parasitic inductance in the transition between the probe tip and the transmission line. Parasitic inductance in the probe-tip-to-transmission-line transition can usually be reduced to negligible levels by moving the reference planes of the two calibrations back to the probe tips. However, parasitic inductance can never be eliminated entirely, and in some situations may even be quite large.

We can understand the first-order effect of parasitic inductance in the transition by adding a series inductance to the circuit of Fig. 2, writing out its cascade matrix X_Z , and eliminating terms that are second order in $Z = R + j\omega L$, the impedance associated with the series parasitic pad resistance R and inductance L . Equation (1) then becomes

$$X_Z = X + \frac{1 - \Gamma}{\sqrt{1 - \Gamma^2}} \left(\frac{Z}{2Z_r} \begin{bmatrix} -1 & 1 \\ -1 & 1 \end{bmatrix} + \frac{ZY}{2} \begin{bmatrix} 1 & \mp 1 \\ \mp 1 & 1 \end{bmatrix} \right), \quad (4)$$

where the negative sign corresponds to placing the pad inductance between the pad capacitance and the impedance transformer, and the positive sign corresponds to placing it before (to the left of) the pad capacitance.

Like the contribution from the pad capacitance, the first new term in (4) cancels from (3), and has no effect on the estimate of Z_0 . This shows a second advantage of the calibration-comparison method for measuring characteristic impedance: to first order the method is insensitive not only to the pad admittance Y , but also to the transition series reactance and inductance Z .

However, the last term in (4) does not cancel from (3), and does, therefore, change the estimate of Z_0 . Substituting the additional last term in (4) into (2) and (3), we derived the estimate

$$\Delta Z_0 \approx \mp ZY Z_r \quad (5)$$

for the error ΔZ_0 introduced into the measurement of Z_0 by the parasitic pad inductance. From (5) we conclude that for pads without significant loss, we can estimate our error as

$$|\Delta Z_0| \sim \omega^2 L |C| Z_r, \quad (6)$$

where we use the symbol \sim to indicate that the error may be on the order of the term on the right, depending on how the inductance is distributed in the pad.

To test the error estimate (5), we applied the calibration-comparison method for measuring characteristic impedance to the coplanar waveguides investigated in [1]. These coplanar waveguides were fabricated on an insulating fused silica substrate, where we are able to apply the more accurate method of [3] to independently measure Z_0 . Figure 3 compares the measurements from the method of [3] to the calibration-comparison method, and shows good agreement.

Figure 3 also compares the estimated characteristic impedance we would obtain from (5) in the presence of an additional inductance of 0.1 nH placed before and after the capacitor (dashed lines). To derive the estimate, we used the value of -6.562 fF for C from [10], set L equal to 0.1 nH, and substituted these values into (5). The value of C is negative here because the capacitance of the pad on the fused-silica substrate is *less* than that of the pad on the gallium-arsenide reference substrate.

We tested these estimates by adding these same inductances numerically either to the left (before the capacitor) or to the right side of X (after the transformer) and then applying the calibration-comparison method. (Since X was measured, we were not able to add the inductance directly between the capacitor and the transformer, as we did in (5).) The results are shown as solid lines in Fig. 3. The figure shows that, while the actual errors are greater than those predicted by (5), the errors in Z_0 are of the same sign and order of magnitude as those predicted by (5).

CONCLUSION

The microstrip lines described in [7] were built on the second level of a six-metal silicon process. This required that via stacks be used to connect the signal line on the second level metal to the sixth (top) level metal. Nevertheless, Fig. 1 shows good agreement between measured and simulated characteristic impedance despite these via stacks and their inductive parasitics.

Reference [11] shows that pad capacitances on the order of 0.04 pF can be easily achieved with “reduced area” designs. If the inductance of the vias in silicon technologies can be kept at 5 pH or below, which we believe is quite easily achieved, we conclude that the error of the calibration-comparison method for measuring characteristic impedance due to parasitic inductance should be on the order of $f^2 \cdot 10^{-3} \Omega$, where f is the frequency in GHz. This indicates that, with careful design, the errors of the calibration-comparison method due to pad inductance and capacitance for measuring characteristic impedance can be made small enough for most applications.

When this level of accuracy is insufficient, we can use estimates of the pad capacitance and inductance and (6) to estimate the error. When the error of the calibration-comparison method for measuring characteristic impedance is too large, the more complex methods of Winkel, et al. [12] or Bracale, et al. [13], which attempt to determine and compensate for parasitic pad inductance, may be appropriate. However, both the methods of [12] and [13] make use of a priori knowledge of the position of the parasitic inductance in the pad model. Fig. 3 and (5) show that we must know, with reasonable precision, how the inductance is distributed in the contact pad before we can accurately correct for its effect on the measured values of Z_0 .

ACKNOWLEDGMENT

We thank Dr. Wojciech Wiatr for his careful reading of the manuscript, the analysis he performed to verify our results, and his observation that the correction for pad inductance depends on the location of that inductance in the pad’s equivalent circuit.

REFERENCES

- [1] D. F. Williams, U. Arz, and H. Grabinski, “Accurate Characteristic Impedance Measurement on Silicon,” *1998 IEEE MTT-S Symposium Digest*, pp. 1917-1920, June 9-11, 1998.
- [2] D.F. Williams, R.B. Marks, and A. Davidson, “Comparison of on-wafer calibrations,” *38th ARFTG Conference Digest*, pp. 68-81, Dec. 1991.
- [3] R.B. Marks and D.F. Williams, “Characteristic impedance determination using propagation constant measurement,” *IEEE Microwave Guided Wave Lett.*, vol. 1, no. 6, pp. 141-143, June 1991.
- [4] Y. Eo and W.R. Eisenstadt, “High-speed VLSI interconnect modeling based on S-parameter measurements,” *IEEE Trans. Comp., Hybrids, Manuf. Technol.*, vol. 16, no. 5, pp. 555-562, Aug. 1993.
- [5] E. Grotelüschen, L.S. Dutta, and S. Zaage, “Quasi-analytical analysis of the broadband properties of multiconductor transmission lines on semiconducting

substrates,” *IEEE Trans. Comp., Packag., and Manufact. Tech.-Part B*, vol. 17, pp. 376-382, Aug. 1994.

[6] W. Heinrich, “Full-wave analysis of conductor losses on MMIC transmission lines,” *IEEE Trans. Microwave Theory Tech.*, vol. 38, no. 10, pp. 1468-1472, Oct. 1990.

[7] U. Arz, D.F. Williams, D.K. Walker, and H. Grabinski, “Asymmetric Coupled CMOS Lines: An Experimental Study,” *IEEE Trans. on Microwave Theory and Tech.*, vol. 48, no. 12, pp. 2409-2414, Dec. 2000.

[8] R.B. Marks, “A Multiline Method of Network Analyzer Calibration,” *IEEE Trans. Microwave Theory Tech.*, vol. 39, no. 7, pp. 1205-1215, July 1991.

[9] R. B. Marks and D. F. Williams, “A general waveguide circuit theory,” *J. Res. Natl. Inst. Stand. Technol.*, vol. 97, no. 5, pp. 533-562, Sept.-Oct., 1992.

[10] D. F. Williams and R. B. Marks, “Compensation for Substrate Permittivity in Probe-Tip Calibration,” *44th ARFTG Conference Digest*, pp. 20-30, Dec. 1994.

[11] D.F. Williams, A.C. Byers, V.C. Tyree, D.K. Walker, J.J. Ou, X. Jin, M. Piket-May, and C. Hu, “Contact-Pad Design for High-Frequency Silicon Measurements,” *2000 Electrical Performance of Electronic Packaging Digest*, Oct. 23-25, 2000.

[12] T.M. Winkel, L.S. Dutta, and H. Grabinski, “An accurate determination of the characteristic impedance of lossy lines on chips based on high frequency S-parameter measurements,” *IEEE MultiChip Module Conference MCMC’96*, pp. 190-195, Feb. 1996.

[13] A. Bracale, D. Pasquet, J.L. Gautier, N. Fel, V. Ferlet, and J.L. Pelloie, “A New Method for Characteristic Impedance Determination on Lossy Substrate,” *2000 IEEE MTT-S Symposium Digest*, pp. 1481-1484, June 11-16, 2000.