A 100 AMPERE, 100 kHZ TRANSCONDUCTANCE AMPLIFIER

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Abstract - A high current, wide band transconductance amplifier is described that provides an unprecedented level of output current at high frequencies with exceptional stability. It is capable of converting a signal voltage applied to its input into a ground-referenced output current up to 100 amperes rms over a frequency range from dc to 100 kHz with a useable frequency extending to 1 MHz. The amplifier has a 1000 watt output capability, ±10 volts of compliance, and can deliver up to 400 amperes peak-to-peak of pulsed current. The amplifier design is based on the principle of paralleling a number of precision bipolar voltage-to-current converters. The design incorporates a unique ranging system controlled by opto-isolated switches, which permit a full-scale range from 5 to 100 amperes. The design considerations for maintaining wide bandwidth, high output impedance, and unconditional stability for all loads are discussed.

I. INTRODUCTION

An ideal transconductance amplifier produces a current in a load proportional to an input voltage and maintains that current independent of the load impedance. This type of amplifier is useful for calibrating and testing instruments and devices requiring a known stable source of current. Although the demand for calibrating devices at high currents and high frequencies is limited, the need is growing. Designers of high-current switching power supplies as well as those researching high frequency welding and bonding techniques are requiring calibrated high current measuring devices. Presently, NIST's calibration service for shunts is limited to 20 A rms and 100 kHz. A transconductance amplifier that will source up to 100 A of current at 100 kHz will serve as an important tool for evaluating the design of new types of shunts and permit the calibration of current measuring devices to a higher regime of current and frequency.

Before discussing the design approach it is essential to realize how the amplifier's output circuit loop-inductance will affect the practicality of the design. This parasitic inductance is considered the worst enemy against achieving the desired performance. The total loop inductance includes all elements in the output circuit loop including the power output stage, internal shunt, output connector, the ground return circuit, as well as the load under test. As little as 12 cm of wire in free-space, regardless of size produces a self inductance of about 100 nH. The goal of producing an output current of 100 A rms at 100 kHz will result in such large rates of change of current that a substantial voltage behind the current source is required to drive the output current through the parasitic output inductance as well as the load impedance. This driving voltage is referred to as the compliance voltage of a current amplifier. The peak compliance voltage required is determined by L(di/dt) where L is the total inductance of the output current loop and di/dt is the maximum current rate-of-change. To appreciate how a design is governed by such constraints, consider for example, a total output inductance of 100 nH and a maximum rate of change of current of about 90 A/μs (the maximum di/dt for a 100 A rms current at 100 kHz). This combination would require a minimum of 9 V of compliance from the amplifier just to overcome the inductance plus some extra, say a total of 12 volts. Thus, for a 100 A capability the amplifier needs to have a 1200 watt capacity with adequate means to dissipate this power while also having a small enough physical geometry to maintain a low inductance in the output current circuit. The requirement for low inductance further dictates that practically all test loads be of a coaxial design. Therefore, a great deal of attention must be given to the geometry of the output circuit to keep the inductance as low as possible. A further problem that arises from the unavoidable power dissipation is the attendant temperature rise which can affect the gain determining elements within the amplifier, thus, compromising output current stability.

II. DESIGN APPROACH

A. The Architecture

While the problems cited above may seem intractable, the principle of the design approach in [1] together with some improvements has made it possible to achieve the design goals. The approach taken is to distribute the total output current capacity of 100 A into twenty individual 5 A voltage-to current

[1]U.S. Department of Commerce, Technology Administration.

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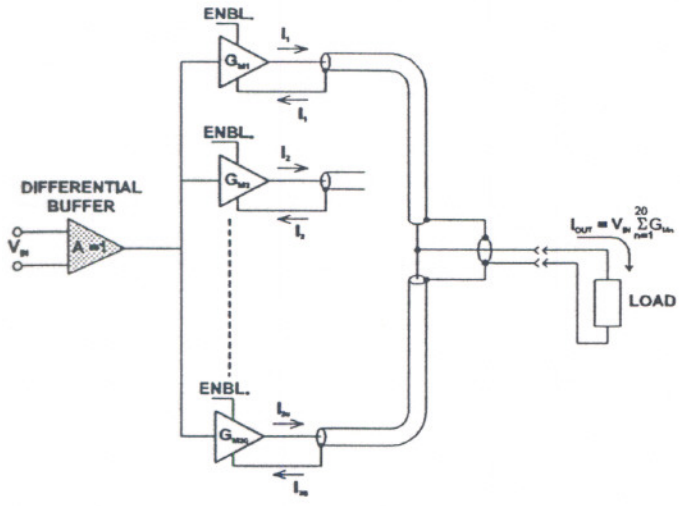

Fig. 1. Block diagram of the high current transconductance amplifier utilizing a parallel array of lower current transconductance amplifiers.

converters connected in parallel, as shown in Fig 1. The paralleled inputs are driven by a differential buffer amplifier. This parallel architecture has several advantages. The total power is evenly dissipated among the individual amplifiers allowing for easier thermal management. A single low-resistance shunt is not required to sense the total output current. The problem of maintaining a low output circuit loop inductance is alleviated by summing the currents at the output connector through equal-length coaxial cables and returning the individual currents to each amplifier, thus, reserving most of the available compliance voltage for the intended load impedance. And finally, by including an enabling feature in each of the amplifiers, a full scale range from 5 to 100 A can be realized by turning on the appropriate number of amplifiers. The total transconductance is the sum of the individual transconductances of the enabled amplifiers. The paralleled approach of course will have a lower overall output impedance than a single unit, but higher currents usually imply a lower load impedance which makes the lower output impedance tolerable.

The differential buffer amplifier that drives the array is essential for separating the voltage input terminal from the common side or ground return of the output load-current terminal. High common-mode rejection of this amplifier will ensure that possible ground loops between input and output are interrupted, an especially important feature when dealing with high output currents at high frequencies. With the parallel approach the problem reduces to designing a 5 A transconductance amplifier that can be paralleled with replicated units.

B. The 5 A Transconductance Amplifier

Fig. 2 shows a simplified schematic diagram of the 5 A transconductance amplifier which provides a ground-referenced output current proportional to an input voltage. The configuration is similar to that reported in [2] but does not rely on precision matched components to provide a high output impedance which, for this application, has proved to be better suited for purposes of paralleling multiple units. Assuming an ideal gain of 1 in the differential amplifier U4, it can be shown that the transconductance G_m, is

$$G_m = \frac{I_{OUT}}{V_{IN}} = \frac{R_2}{R_1 R_S}\left[\frac{1}{1 + \frac{R_1+R_2}{R_1}\cdot\frac{1}{A(\omega)}}\right] \qquad (1)$$

where $A(\omega)$ = Total open-loop voltage gain.

For a large open-loop gain, G_m reduces to a dependence of only resistors R_1, R_2, and R_s while the 3-dB bandwidth is determined by the frequency where $A(\omega) = (R_1+R_2)/R_1$. Amplifier U1 provides the major portion of the loop gain and the discrete devices (Q1-Q6) provide current gain between U1 and the output. Also, the circuit provides a ground-referenced voltage proportional to the output current. The usefulness of this feature will be discussed later.

This design takes advantage of a relatively new high-speed, video difference amplifier, U4, to amplify the signal across the shunt, R_s, and to produce an output voltage that is fed back through R_2 where it is compared with the input voltage at the summing junction of U1. The particular difference amplifier that is used at a gain of 1 has a typical 3 dB bandwidth of 100 MHz. With such a wide bandwidth it is possible to neglect its effects in the feedback loop. Moreover, it has an outstanding common-mode rejection ratio (CMRR) that is typically 100 dB out to 200 kHz and drops only to 60 db at 4 MHz. As will be discussed further, it is the CMRR that has the most dominant effect on the output impedance. The influence of the dc input offset drift of U4 is effectively canceled by the similar drift characteristics of a second differential amplifier, U2, connected to the non-inverting input of U1. Both devices are coupled by a low thermal resistance to improve tracking. This technique improves the dc output current drift of the amplifier to better than 50 μA/°C.

The quality of the shunt resistor R_s, used to sense the output current has a direct bearing on the overall accuracy, stability, and bandwidth of the amplifier. In Fig. 2 R_s, is a four-terminal shunt employing the design described in [2]. The shunt was constructed from 100 10-ohm metal-film resistors stacked in a square array between two double-sided copper circuit boards to form a nominal 0.1 Ω resistor. The outer copper surface of each board serves as the input and output current terminal, and the potential terminal is

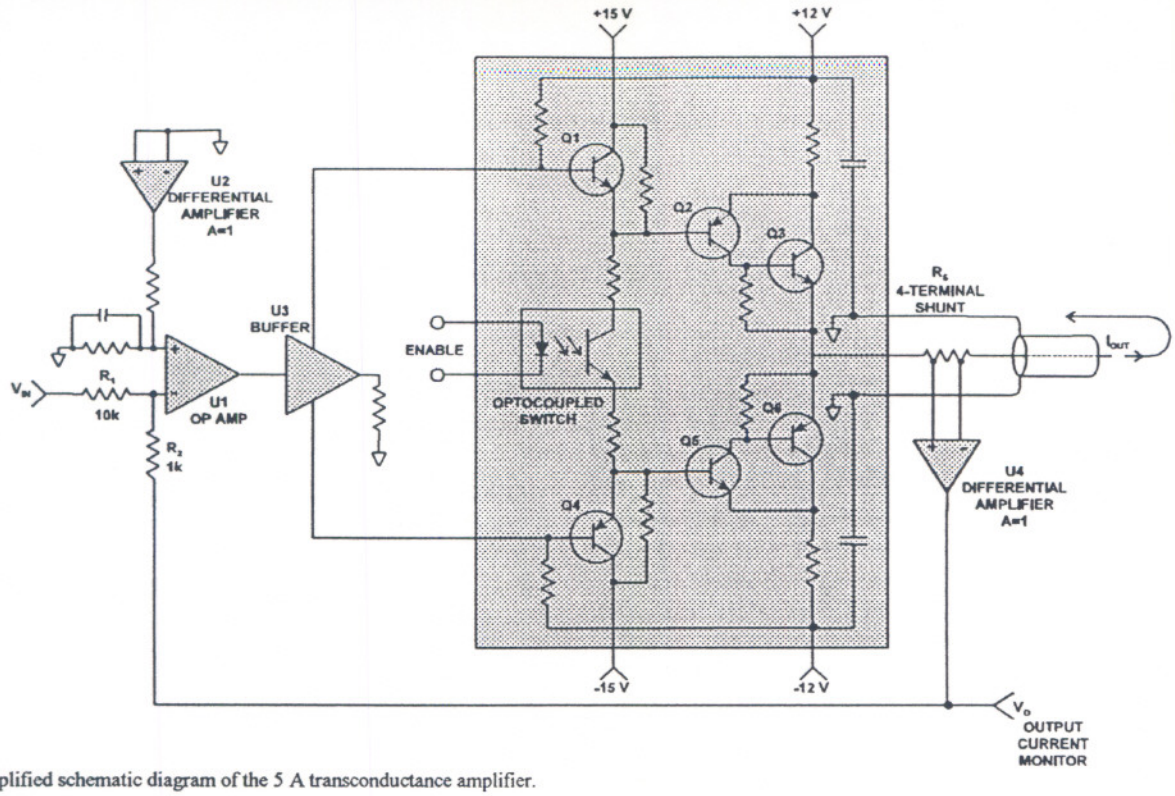

Fig. 2. Simplified schematic diagram of the 5 A transconductance amplifier.

connected to the respective inner copper surfaces of the boards at the center of the resistor matrix. This design is relatively inexpensive and exhibits an impressive combination of performance features. The individual resistors used for the shunt were specified with a ±25 ppm/°C temperature coefficient of resistance (TCR), but measurements of 25 fabricated 0.1 Ω shunts showed that all units exhibited a TCR under ±5 ppm/°C. The free-air thermal resistance of the shunt is about 4 °C/W resulting in a power coefficient of resistance of 20 ppm/W. The ac-dc differences of the shunt were determined at 5 A from the difference between the alternating current required for a given output emf and the average of both polarities of direct current required for the same emf. Table I shows the results of differences expressed in parts per million (ppm), where a positive sign indicates that more alternating current was required to produce the same emf.

A power gain between the output of U1 and the output current I_{out}, was implemented with a buffer amplifier serving as a polarity splitter and with discrete components providing the major portion of current gain and drive capacity. The output stage is a class AB full-complementary-symmetry driver with an overall current gain of about 700 designed to operate at an output current up to 10 A. In the actual implementation Q3 and Q6 are each paralleled with four additional transistors to provide additional current gain and to better distribute the power to the heat sink. The output stage must be able to dissipate up to 60 watts of power. Low crossover distortion is assured by including base-emitter resistors on Q3 and Q6 and operating the output stage at a quiescent current of about 800 mA. The quiescent current is fixed by the quiescent current of buffer amplifier U3 and the current gain of the output stage. Also, the output stage is controlled by an enable input which activates an opto-coupled switch. When the switch is turned off the base-emitter junctions of Q1, Q2, Q4, and Q5 are reverse biased which completely turns off the output stage, thus, blocking any forward signal from appearing at the output. The only effect of the amplifiers in the off condition is the shunting effect of the inter-electrode capacitances of the output transistors tending to lower the output impedance.

The two principle design considerations for the transconductance amplifier is the accuracy and flatness of the forward transfer function (G_m) and the output impedance (Z_0). It is fairly easy to achieve acceptable gain-flatness by employing sufficient loop gain with well behaved phase characteristics insured by a dominant

TABLE I
AC/DC Difference Determinations of 0.1 Ω Four-Terminal Shunt

Current Range	Applied Range	Ac-dc Difference (ppm)					
Amperes	Amperes	100 Hz	1 kHz	10 kHz	20 kHz	50 kHz	100 kHz
5	5	+3	+4	-1	+24	+121	+271

pole. However, maintaining a high output impedance particularly at high frequencies is much more difficult. When the output impedance is too low in relation to the load impedance, the current will divide between the output impedance and the load impedance. This division makes it particularly difficult to determine an overall effective transfer function that is independent of the load impedance. Here again, it must be remembered that in practice a significant part of the load impedance includes a parasitic load inductance. Maintaining a high output impedance that is several orders of magnitude greater than the load impedance over the bandwidth of the amplifier is the greatest challenge. It can be shown that the equivalent output impedance, Z_o, of the amplifier in Fig. 2 can be expressed as

$$Z_o = \frac{R_S}{1 - \frac{(1 - \frac{1}{K(\omega)})}{1 + (\frac{R_1 + R_2}{R_1})\frac{1}{A(\omega)}}} \qquad (2)$$

where $K(\omega)$ = CMRR of differential amplifier U4
$A(\omega)$ = Total open-loop voltage gain.

Equation (2) shows that both the frequency dependent CMRR and open-loop gain play a dominant role in controlling the output impedance. Because these terms are both complex quantities there is always the risk that the real part of Z_o will become negative over some frequency range. In fact, one of the reasons some transconductance amplifiers tend to oscillate with inductive loads is that the real part of the output impedance becomes negative over a certain frequency range. Computer simulation is the most practical way of examining the output impedance. When there is a tendency toward negative output impedance, usually the excess phase shifts in the open-loop gain are to blame. Compensating the open-loop phase and/ or decreasing the CMRR are effective ways of manipulating the complex components of the output impedance. Even if $A(\omega) \rightarrow \infty$, then $Z_o \rightarrow KR_s$, which for a CMRR = 100 dB yields a maximum output impedance of 10 kΩ. As the frequency increases the effect of the poles in $K(\omega)$ and $A(\omega)$ will cause the output impedance to drop at the rate of 12 dB per octave.

III EXPERIMENTAL RESULTS and DISCUSSION

Twenty 5 A-transconductance amplifier units described in section IIB were fabricated and assembled in the parallel arrangement of Fig. 1. Each amplifier was designed as a modular unit with its own heat sink and input/output connections. The entire modular array is cooled by forced air and powered by two 12 V, 150 A switching power supplies. In lieu of coaxial cables, 45 cm long flat flexible circuit material with 6.3 mm wide 2 oz. copper traces separated by a thin dielectric were fabricated for the output conductors. The total inductance and capacitance of an individual conductor was measured to be about 50 nH and 500 pF, respectively.

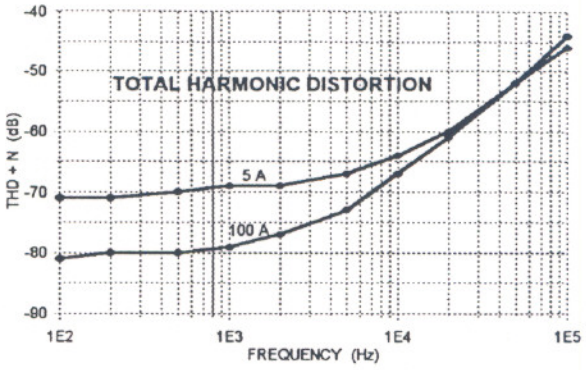

Fig. 3. Plot of total harmonic distortion plus noise vs frequency.

A differential buffer amplifier (see Fig. 1) was designed with the appropriate bandwidth and current capacity to drive up to 7 V rms into the inputs of the parallel array. A ranging system was devised so that a range from 5 to 100 A in 5 A increments is provided by turning on the appropriate number of amplifiers. Programmable logic devices were used to control the enable inputs of each amplifier in an up-down fashion similar to a bar display driver. A "dot mode" can also be implemented to turn on any one of 20 amplifiers for test purposes.

Fig. 3 plots the total harmonic distortion plus noise (THD+N) vs frequency for the 5 A and the 100 A range. Measurements were made with a commercial audio distortion analyzer. A current transformer was used to measure the output current on the 5 A range and a 5 mΩ wide band shunt was used for the 100 A range. The almost 10 dB improvement at lower frequencies for the 100 A output over the 5 A output is surmised to be due to the random noise reduction that changes in inverse proportion to the √N, where N is the number of amplifiers in parallel. Because the overall harmonic distortion performance is more that adequate the conjecture was not tested.

The magnitude of the output impedance of the complete amplifier was measured on the 5 A range. That is, one amplifier turned on and the 19 others turned off. A wide band in-line current transformer was used to measure the change in output current when the load was changed from a short circuit (≈ 0 Ω) to a known resistance (1 Ω). The output impedance was computed by dividing the known resistance by the percent change in output current at each test frequency. The results are shown dotted in Fig. 4. Note the rapid decline in output impedance above 2 kHz to about 20 Ω at 100 kHz. The measured decline in output impedance with frequency follows the prediction of equation (2) fairly well, provided an additional capacitance of about 20,000 pF is included as part of the output impedance. This additional capacitance comes from the inter-electrode capacitances of the output amplifier stages that are turned off and the capacitance of

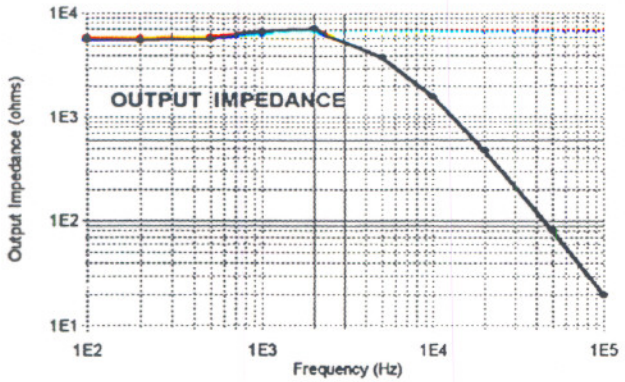

Fig. 4. Plot of output impedance vs frequency on the 5 A range.

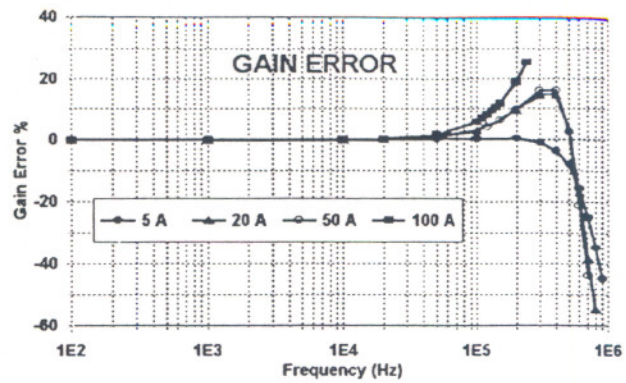

Fig. 5. Plot of gain error vs frequency for four ranges.

the flat cabling which connects each of the amplifiers to the output connector. At the 100 A range the output impedance can be expected to be 1/20th the values of Fig. 4 or about 1 Ω at 100 kHz. While a typical load resistance at 100 A may be in the order of a few milliohms, it is the unavoidable parasitic load inductance which raises the total load impedance so that it is no longer insignificant in relation to the output impedance. The parasitic output inductance due to the output connector and fixturing was determined at about 50 nH. Thus, at 100 kHz the 50 nH inductance contributes another 30 mΩ to the total load impedance, which is a significant percent of the output impedance.

While the magnitude of the output impedance is predominantly capacitive, the real part of the output impedance appears to be positive over the entire bandwidth, as evidenced by an unconditional stability for all types of loads on all ranges, particularly inductive types.

Fig. 5 shows the gain error of the amplifier on four ranges up to 100 A. The purpose of this plot is to show how the gain error is affected by the range setting at the higher frequencies. Note that on the 5 A range the response is reasonably flat, but as the range increases the peaking gets higher. This effect is due to the formation of a low Q resonant circuit at the amplifier output by the output impedance and the parasitic load inductance. On the higher ranges the output impedance is lower (a larger effective capacitance) which lowers the resonant frequency. What is being observed is a rising inductive current below the resonant frequency. The increasing inductive current with frequency is either limited by the forward gain roll-off or the compliance voltage of the amplifier. Although not shown in the Fig. 5, the gain error for all ranges is under ± 0.1% up to 10 kHz for loads below 0.5 Ω per ampere of range.

The problem of low output impedance at high frequencies causing the output current to be load dependent can be attacked in two ways. As equation (2) shows, a differential amplifier would be required with at least a CMRR = 120 dB at 100 kHz and the loop gain of the amplifier would also need to be raised to gain about an order of magnitude in output impedance. Such requirements are difficult to attain. The other approach is to compensate for the transconductance amplifier's insufficient output current regulation by measuring the load current and appropriately changing the input voltage in some type of software control loop. One possibility of accomplishing the current measurement within the amplifier is to sum the voltage output of differential amplifier (U4) in Fig. 2 of each transconductance amplifier. Because the responses of the differential amplifier and shunt resistor are quite flat, this would obviate the need for an external (to the amplifier) current measuring device. The problem then remains to accurately sum the output voltage from each amplifier, determining the rms value, and devising a control loop to reprogram the input voltage. This compensation scheme would benefit those applications requiring a known source of current that is independent of the load impedance. This scheme is presently under investigation.

IV CONCLUSIONS

A high current, wide band transconductance amplifier has been described that is capable of providing a ground-referenced output current up to 100 A rms over a frequency range from dc to 100 kHz. The design is based on paralleling an array of twenty 5 A transconductance amplifiers. Each amplifier of the array can be turned on or off by an enabling signal, which thereby provides a full scale current range from 5 to 100 amperes. The parallel structure avoids the need for a single high-current shunt and significantly lowers the output parasitic inductance, allowing for a practical level of compliance voltage. Measurements on a prototype amplifier show that at full output current the total harmonic distortion is better than -60 dB at 20 kHz and drops only to -45 dB at 100 kHz. Analysis and test results show that falling output impedance with frequency is the primary cause for higher

gain error at high frequencies. A method of compensating for gain error is proposed.

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